MADEin4

Wafer Inspection and Metrology Challenges and Innovations for Advanced Semiconductor Technology Nodes

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Applied Materials Israel Ltd.

September 15, 2022

AGENDA

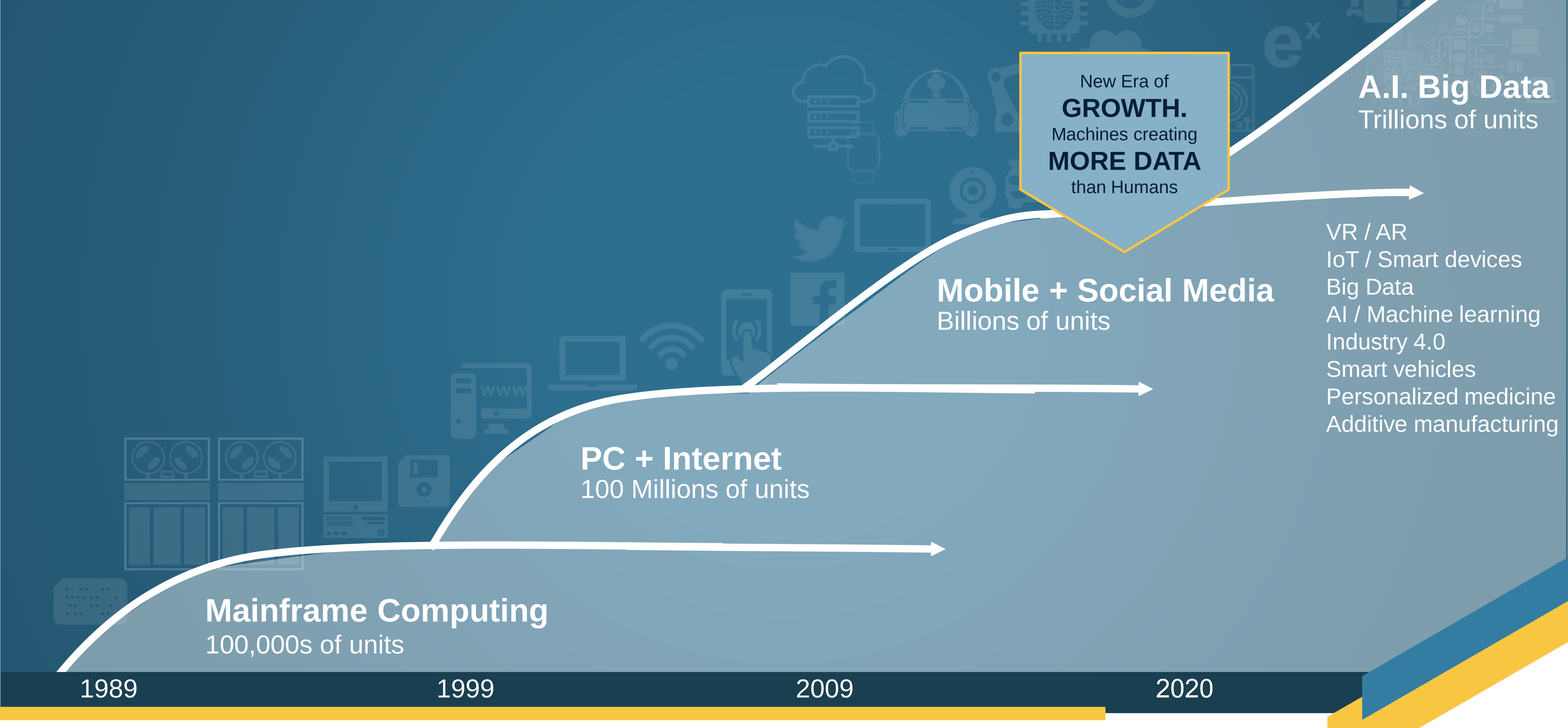
Metrology and Inspection Challenges – Background

Applied Materials Israel Main Tasks in MADEin4

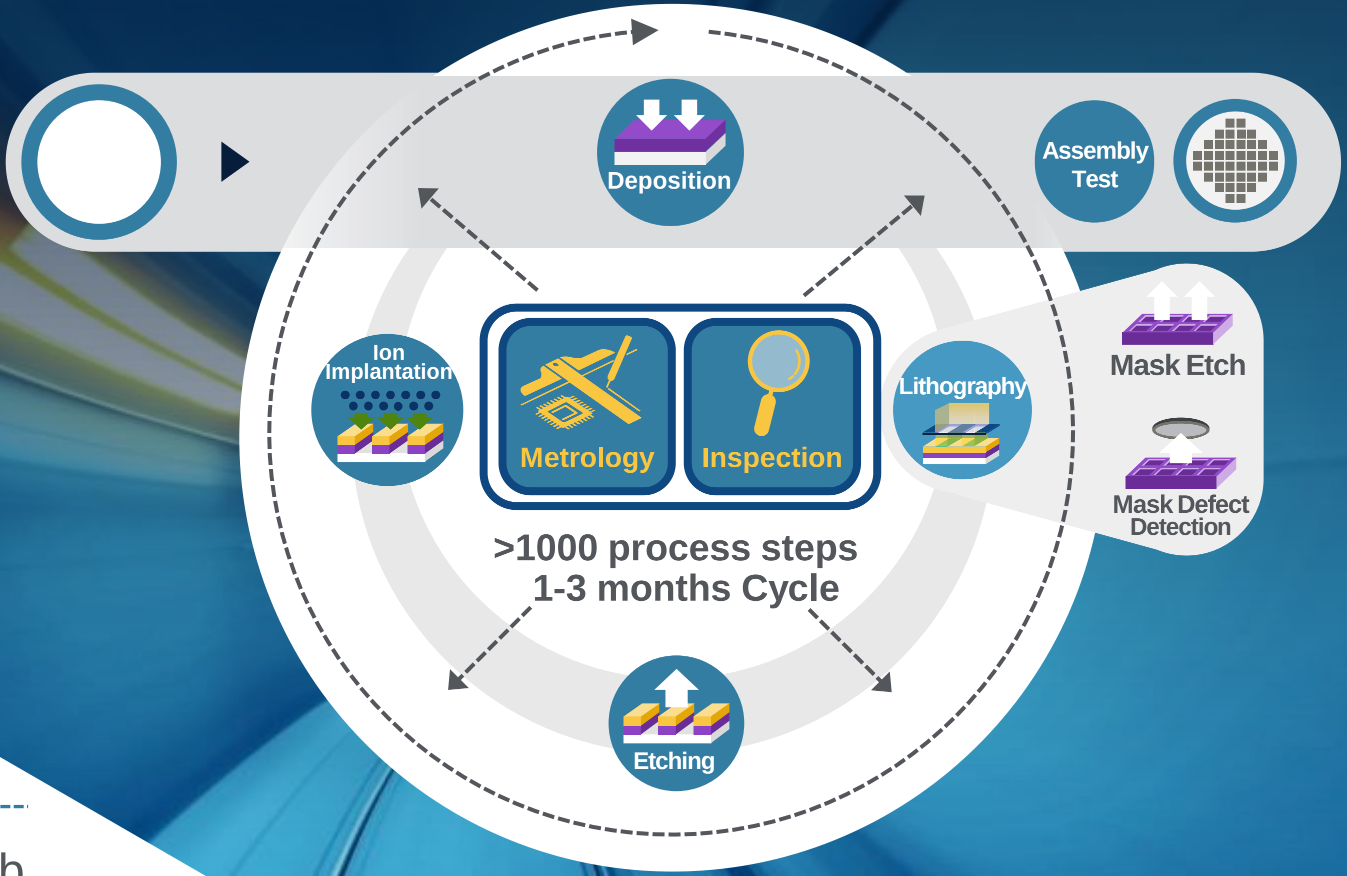
Summary

APPLIED MATERIALS®

Golden Era for Semiconductors – Demand and Drivers



Metrology and Inspection – Time to Market Acceleration



"Time is money?"
This is HOW MUCH...

At DRAM fab one week downtime equals ~**2% annual revenue** plus ASP erosion.

At 3nm logic fab, one week of downtime results in **$25 million** cost.

Process Diagnostics and Control

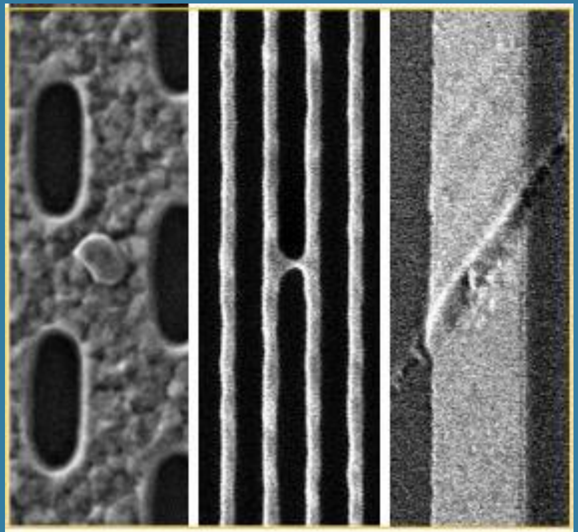
We are the fab's eyes

We work in the forefront of technology to provide the wafer fab industry with **Patterning Control** and **Defect Control** cutting edge solutions

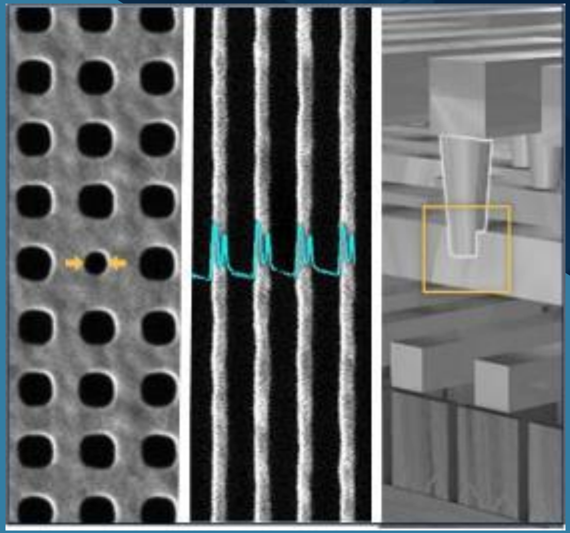
Metrology and **Inspection** enables chip manufacturers see clearly into their process and accelerate time to market of their most advanced technologies

- **Detect & Classify**
- **Measure**
- **Characterize**

Defect Control
Killer defects should **NOT** exist on the wafer



Process stability
Yield enhancement and control

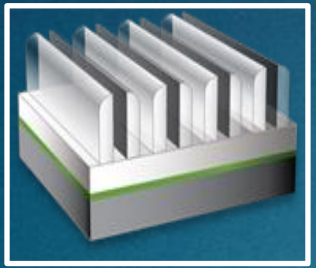


Patterning Control
Minimize deviations of structures that **SHOULD** exist on the wafer

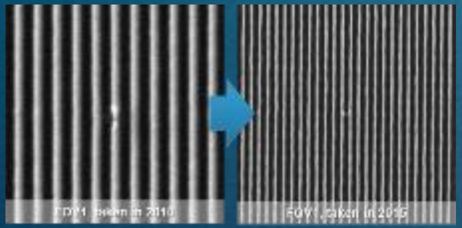
Source: Applied Materials

There are Many Metrology and Inspection Challenges

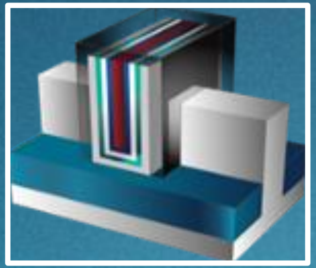
Design Rule Shrink



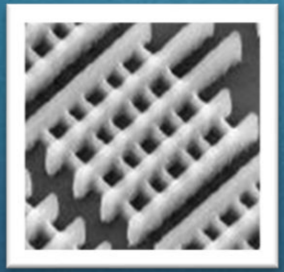
- Denser features imaging
- Smaller defects become killers



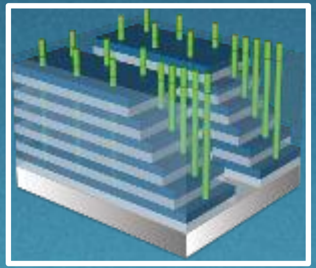
3D Transistors



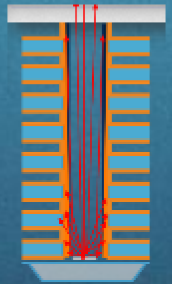
- Complex geometries, trenches, sidewalls
- New materials
- No line of sight



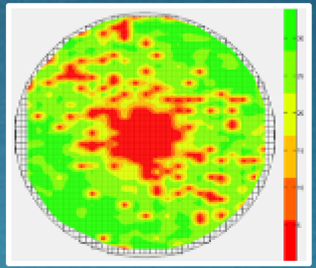
High Aspect Ratio



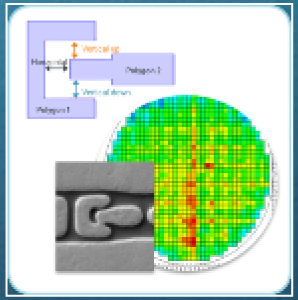
- Metrology challenges due to HAR geometry
- Buried defects



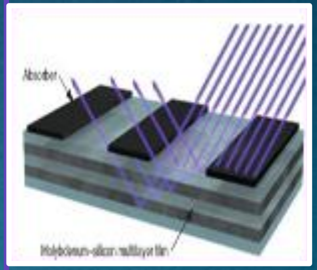
Process Marginality



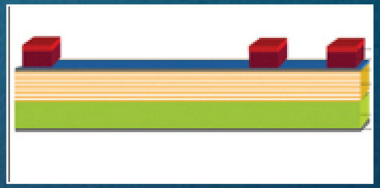
- Systematic defects
- Insufficient metrology coverage



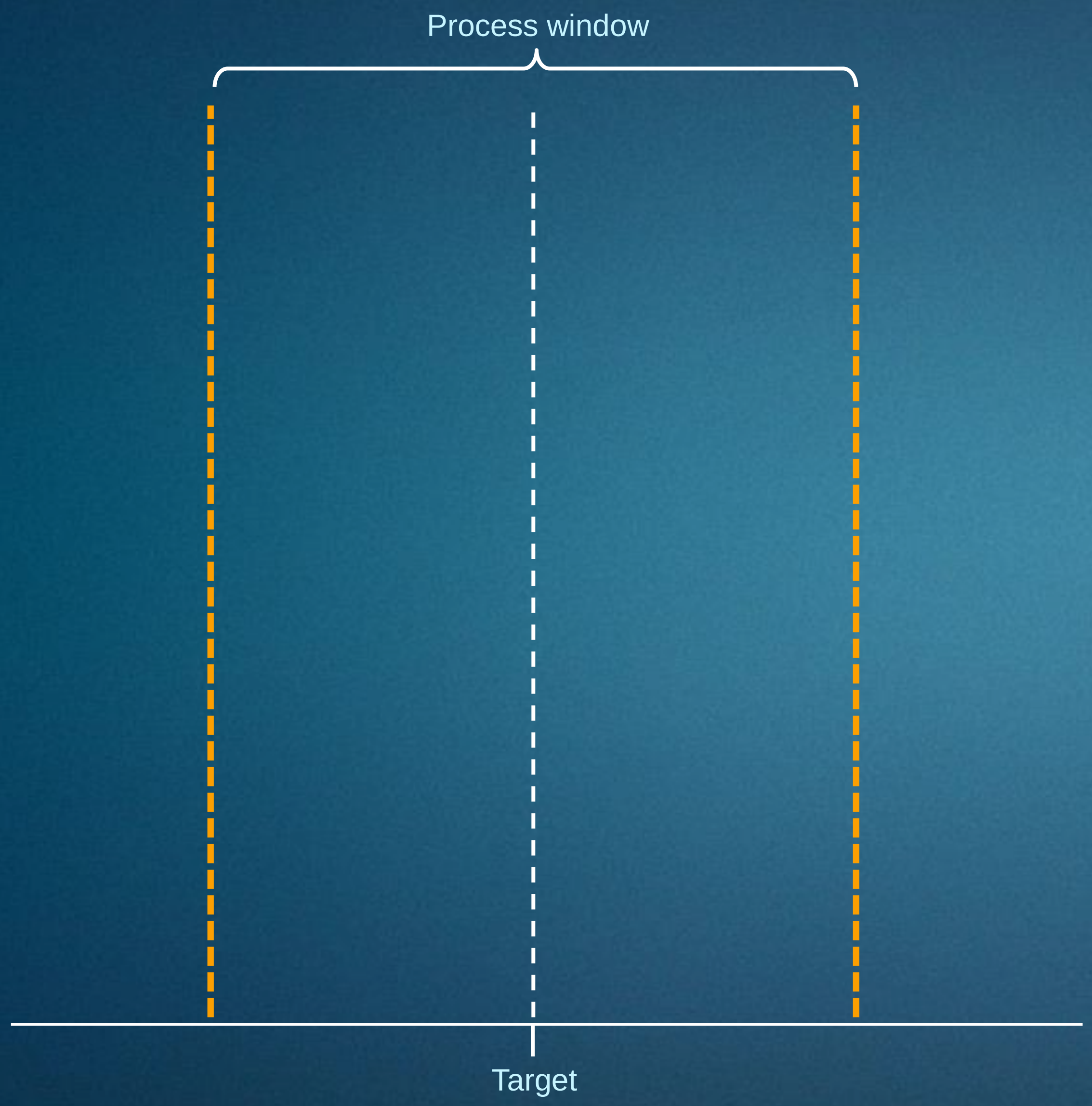
EUV Lithography



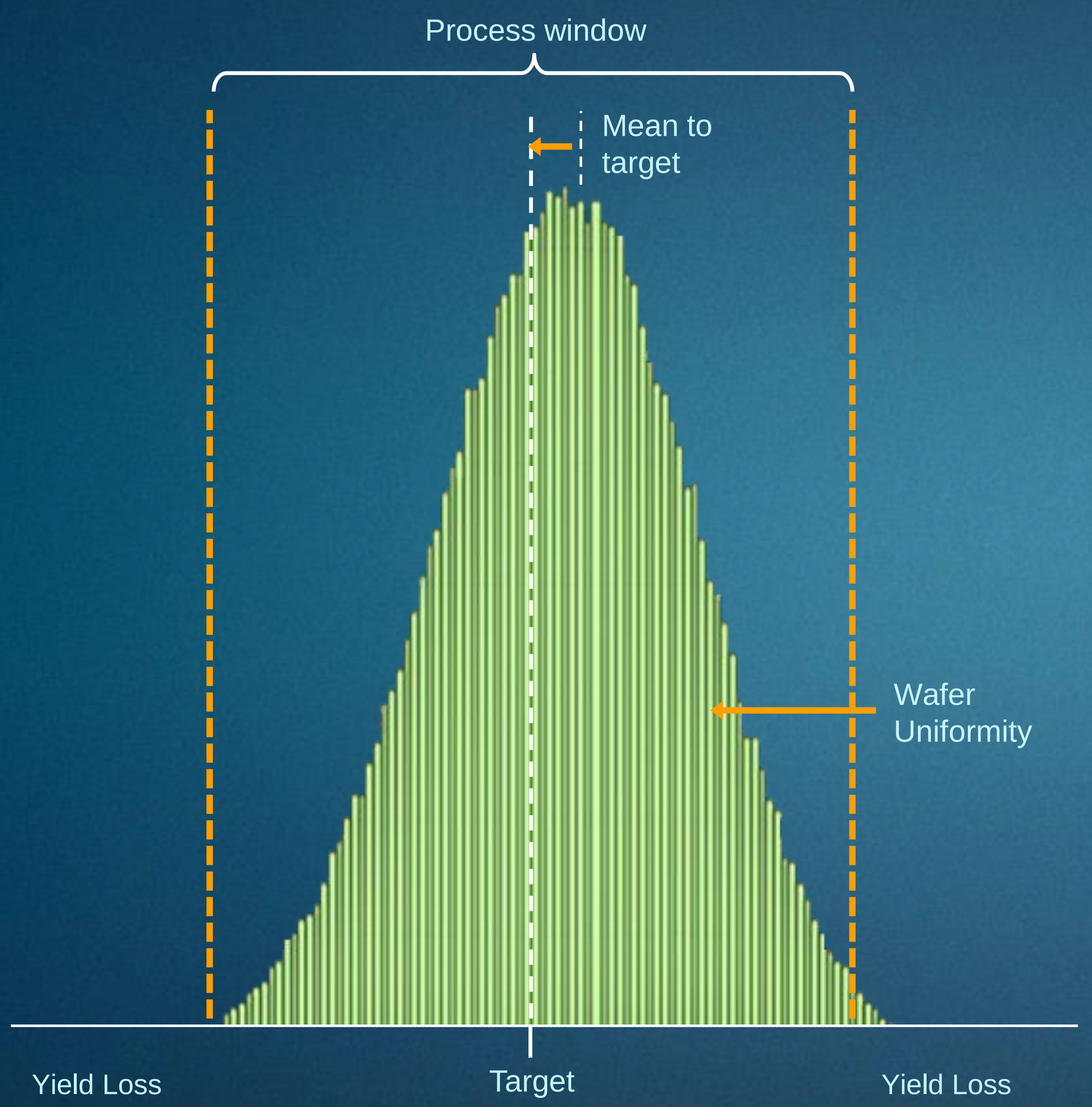
- New mask technology
- Sensitivity requirements



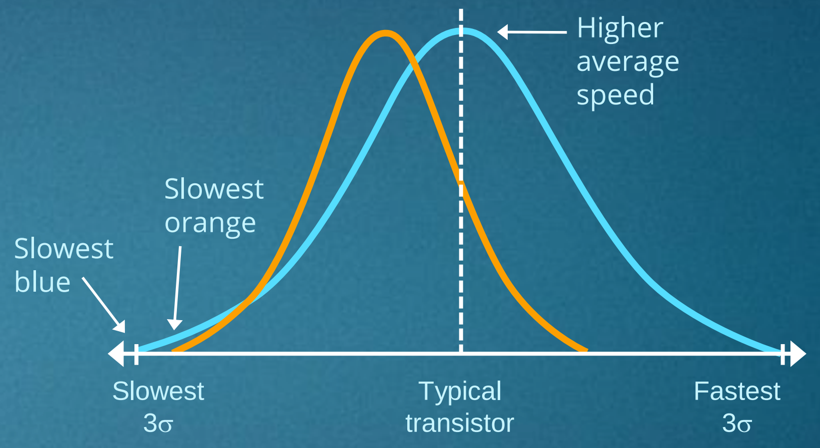
Process Control – Metrology and Defectivity



Controlling Mean and Mean Variation of a Parameter



Variability implication – circuit performance example

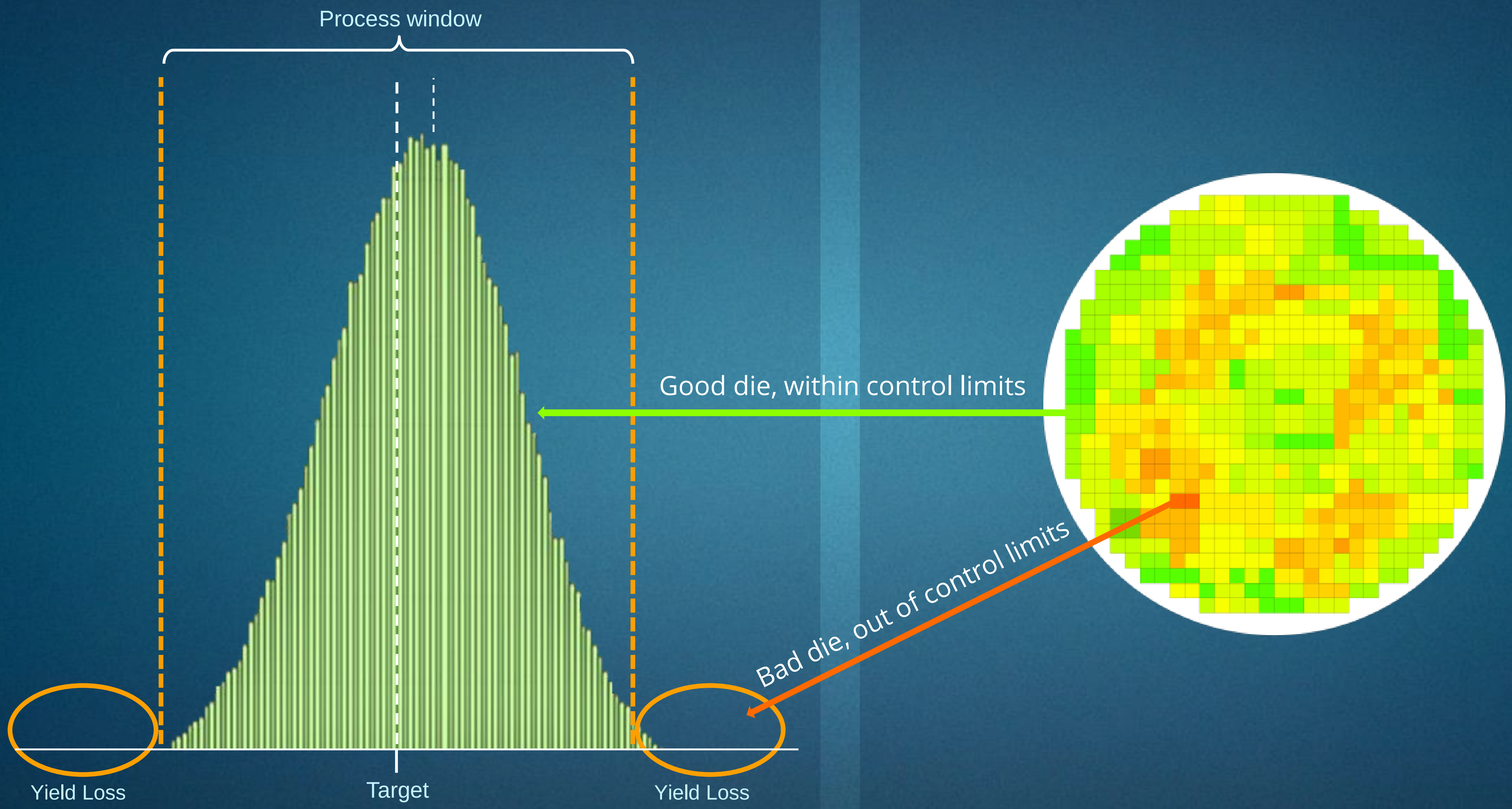


Greg Yeric, IEDM 2015

Circuit performance is gated by the slowest transistor

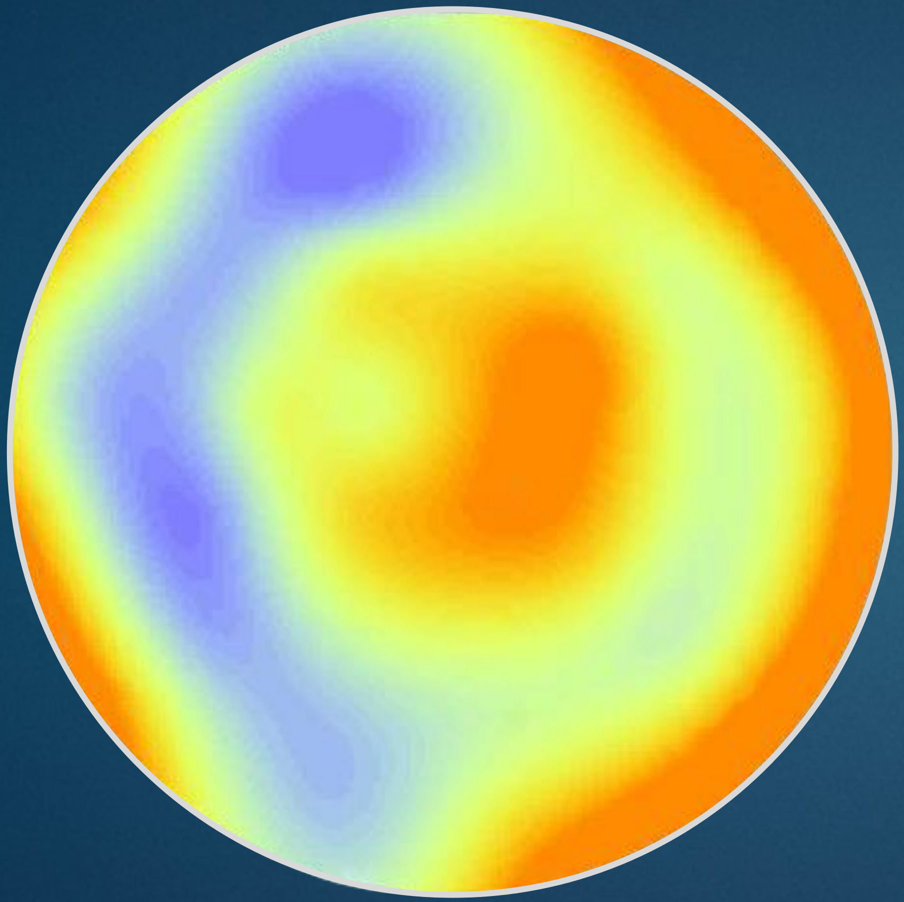
Lower transistor variability
= higher device performance

Maintaining Process Window



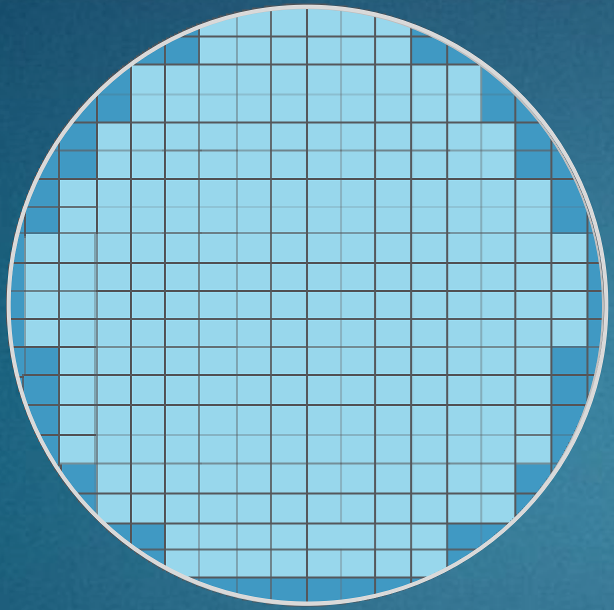
APPLIED MATERIALS

Process Steps Introduce Variations Across the Wafer

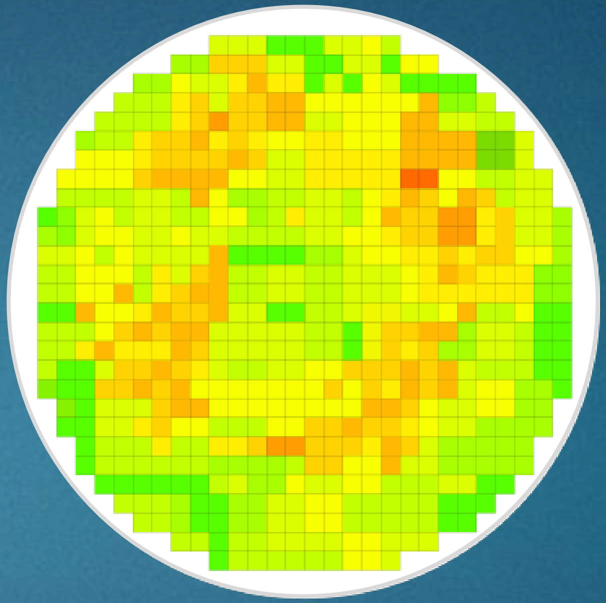


Source: Chipworks

From Statistical Sampling to Massive, Across-wafer Sampling

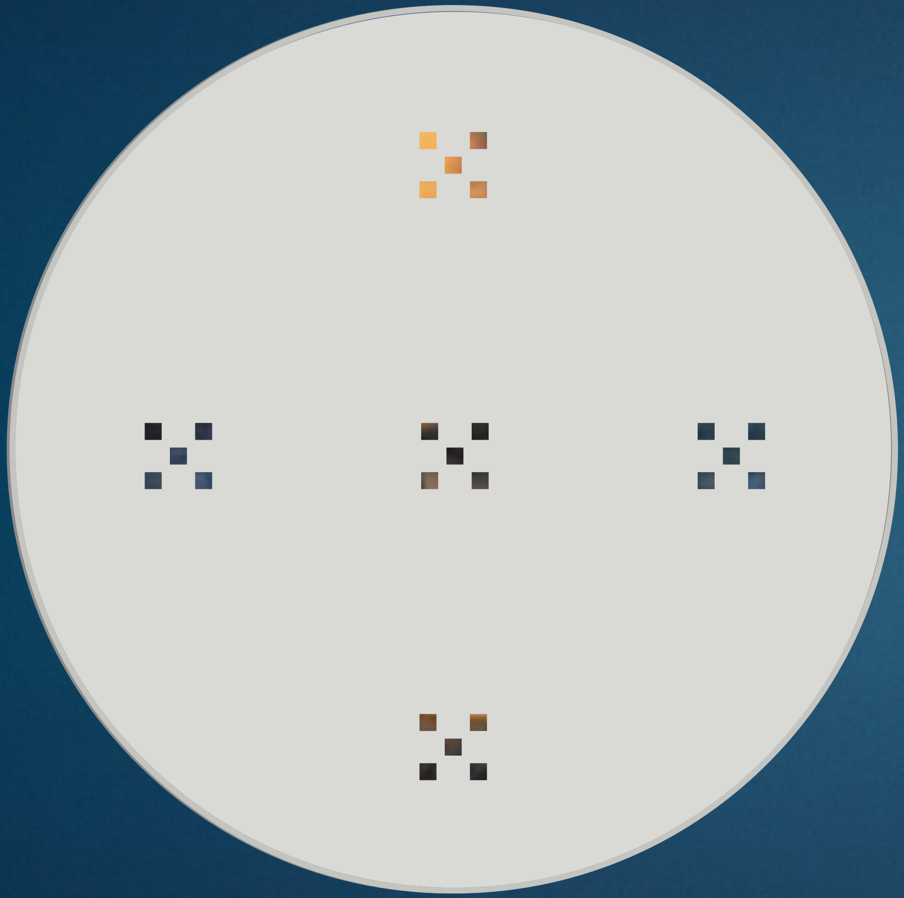


Statistical sampling



Massive metrology and inspection

From Statistical Sampling to Massive Sampling



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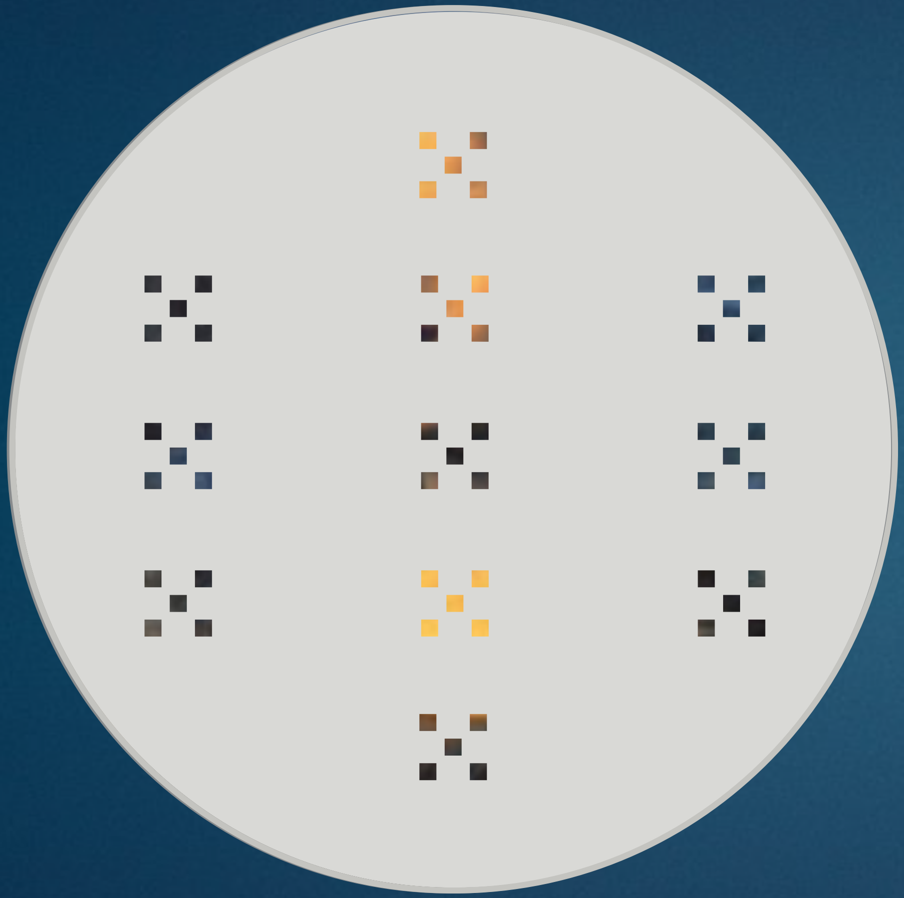

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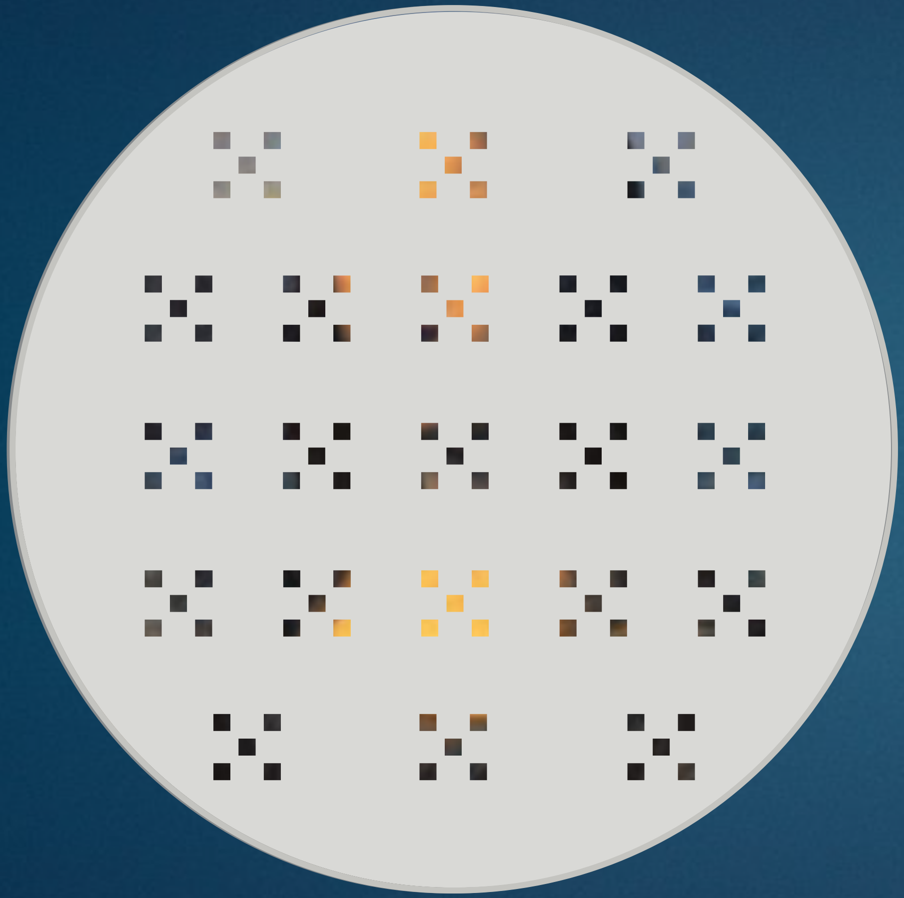

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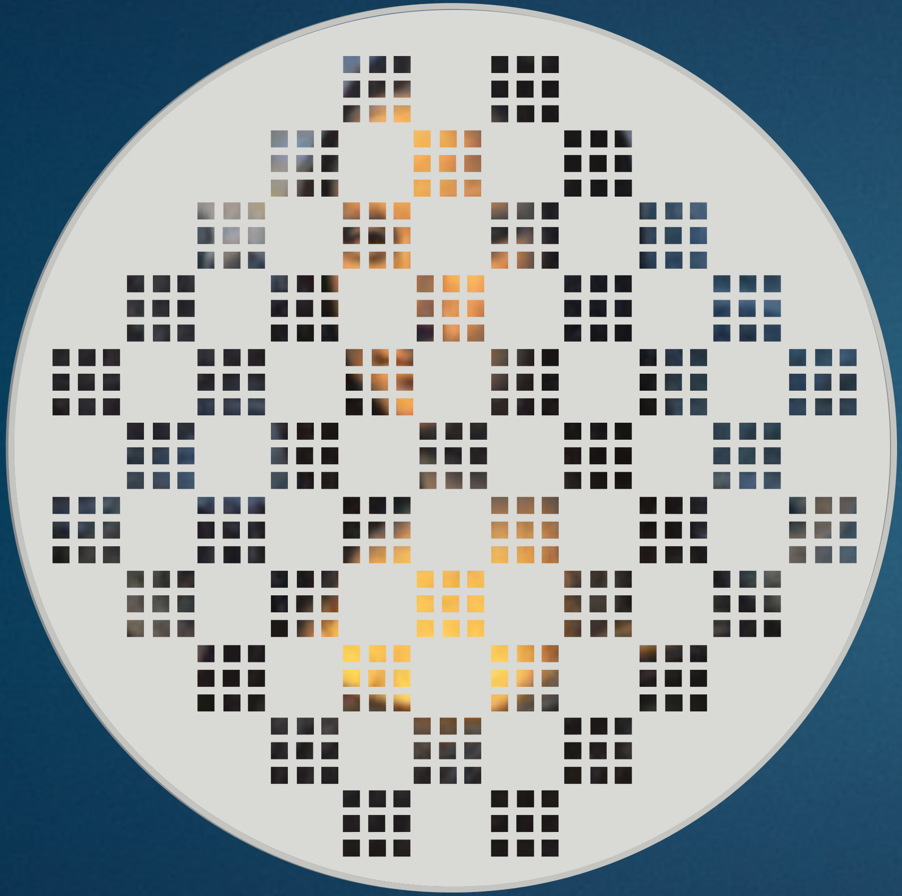

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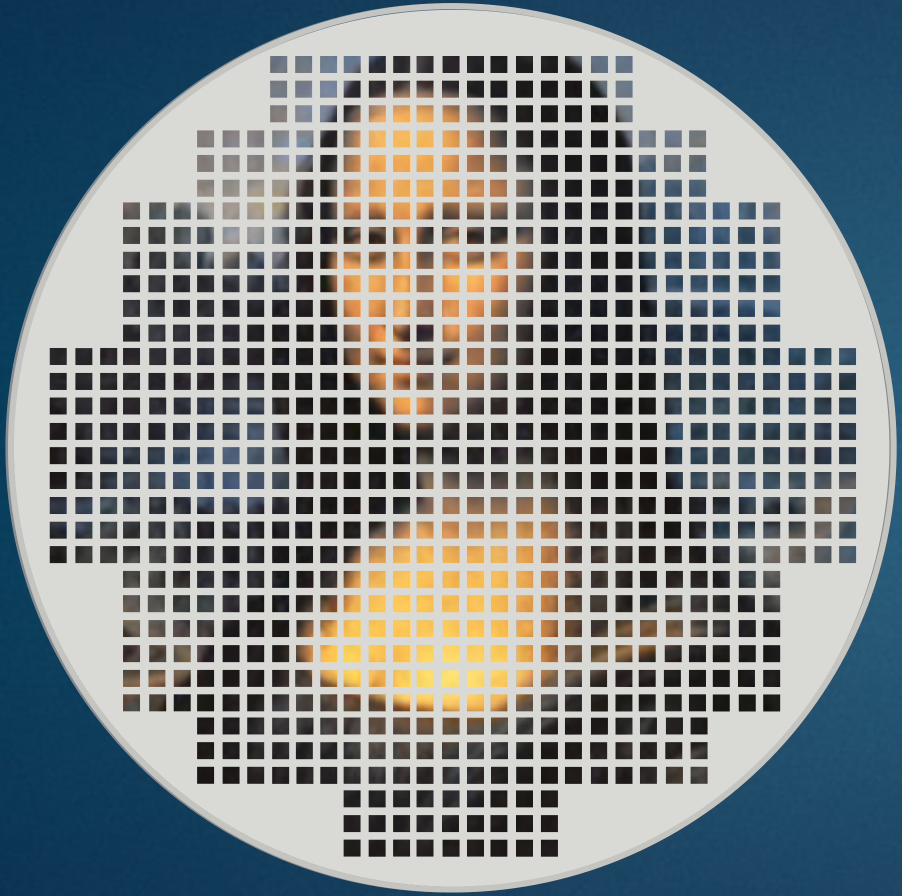
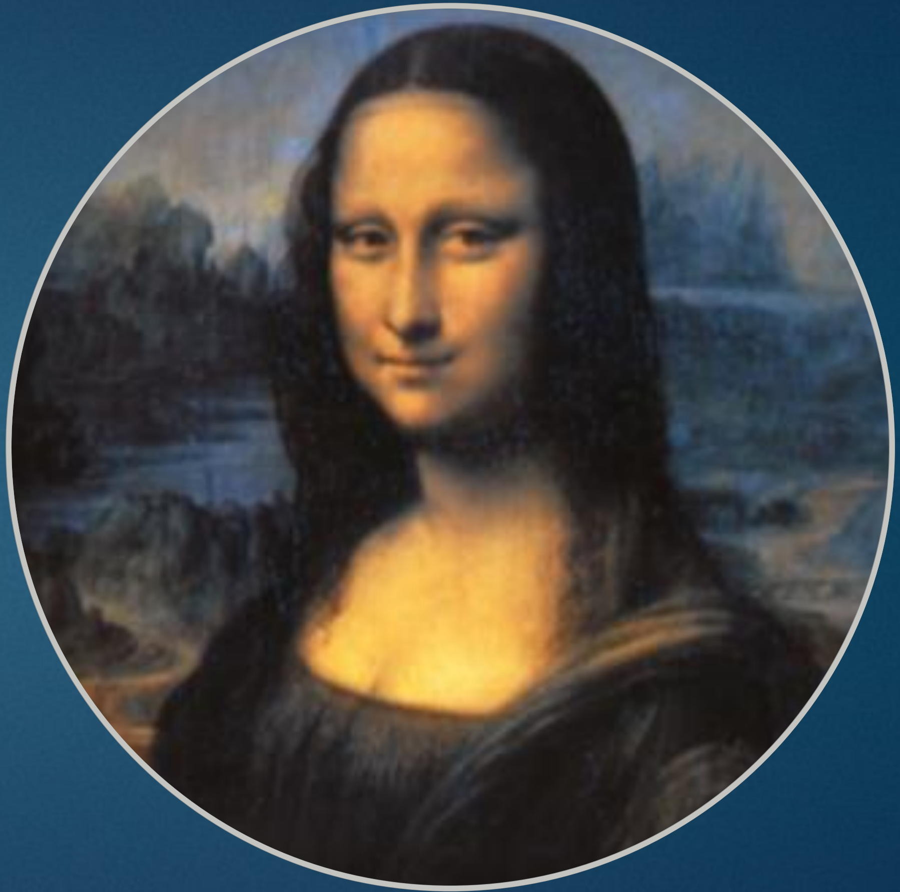
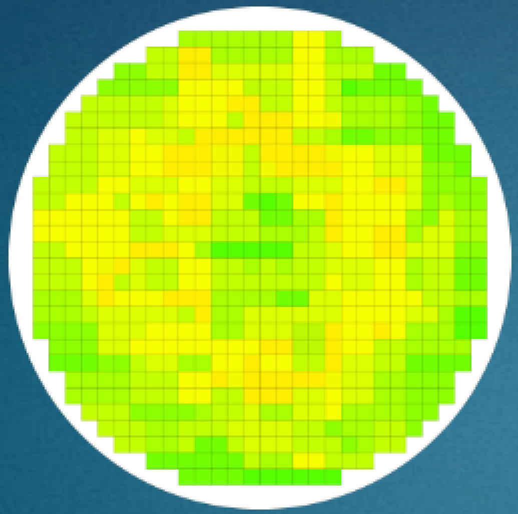




Massive sampling reveals hidden information

Massive Sampling Reveals Process-Induced Issues



Sparse sampling

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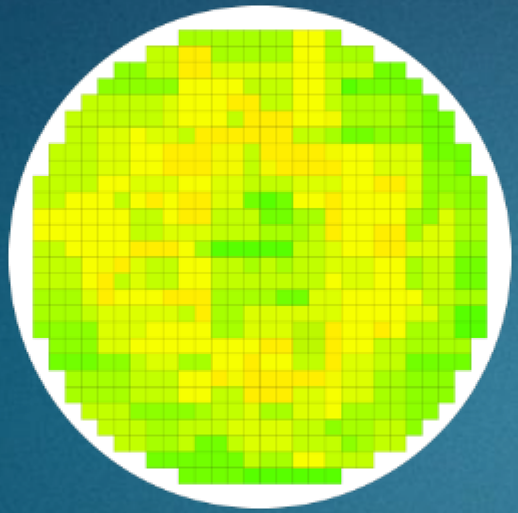

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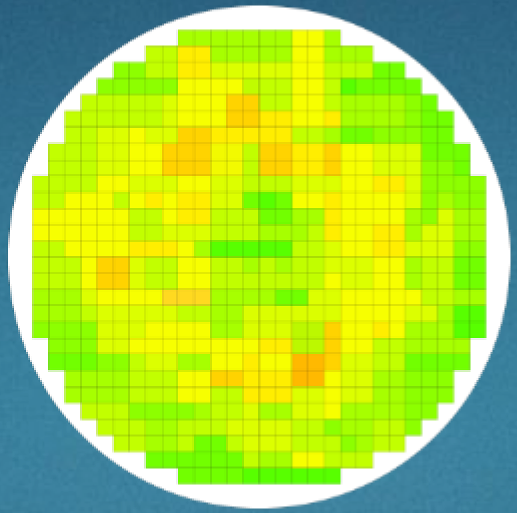

Massive sampling reveals process signature

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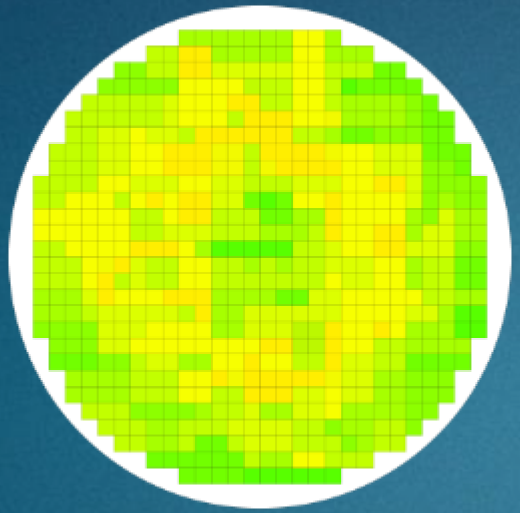

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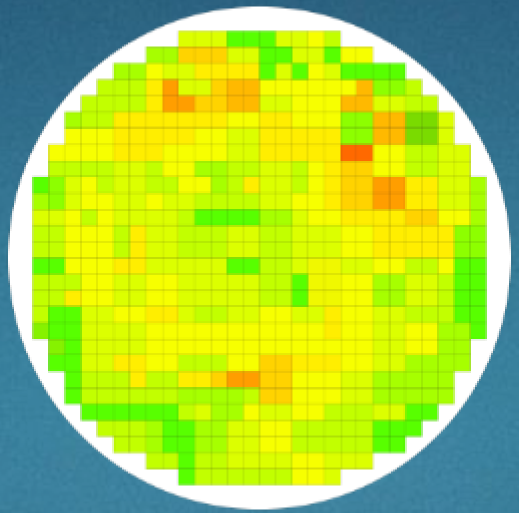

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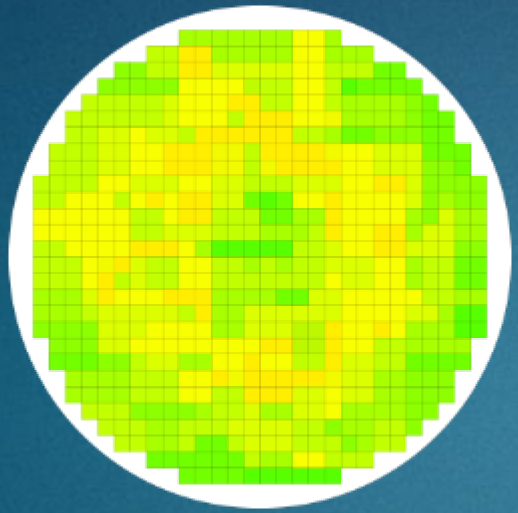

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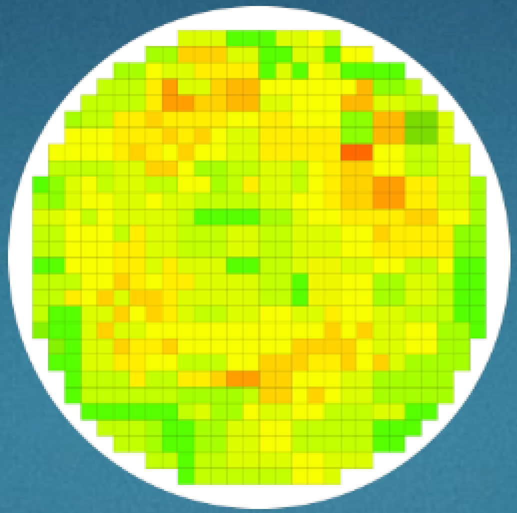

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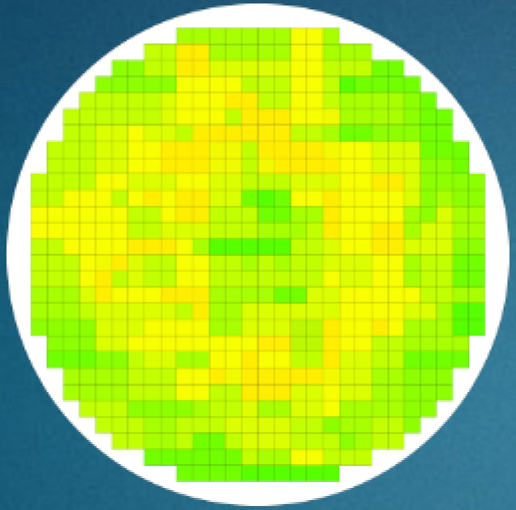

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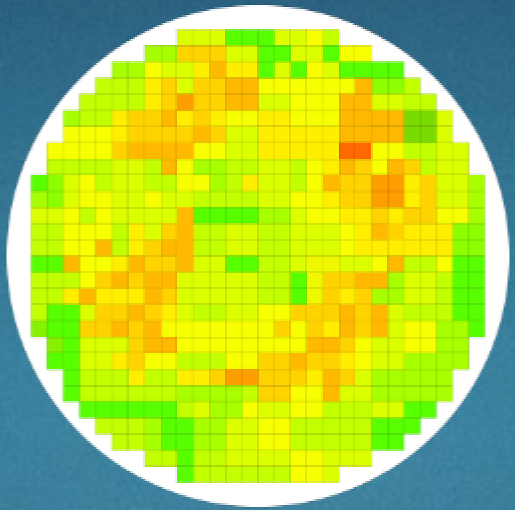

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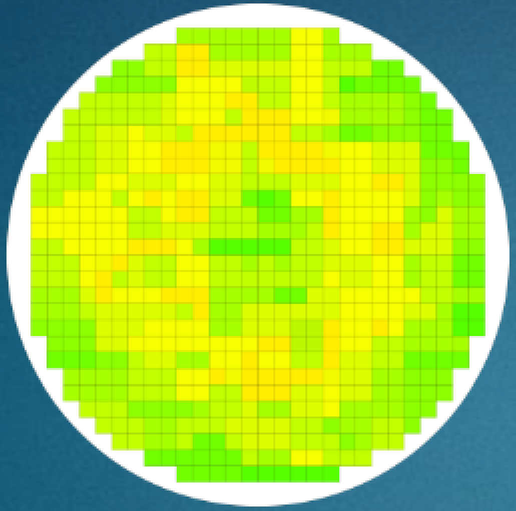

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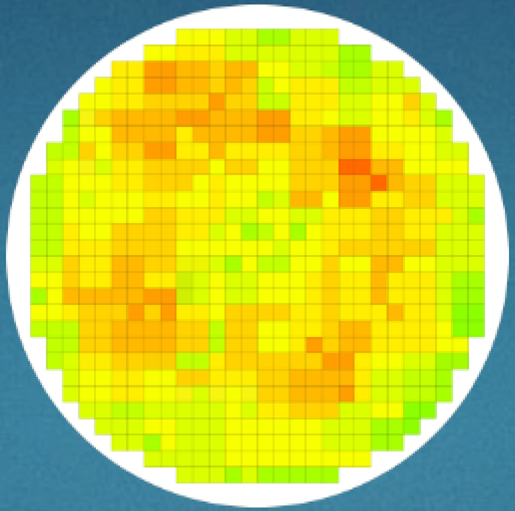

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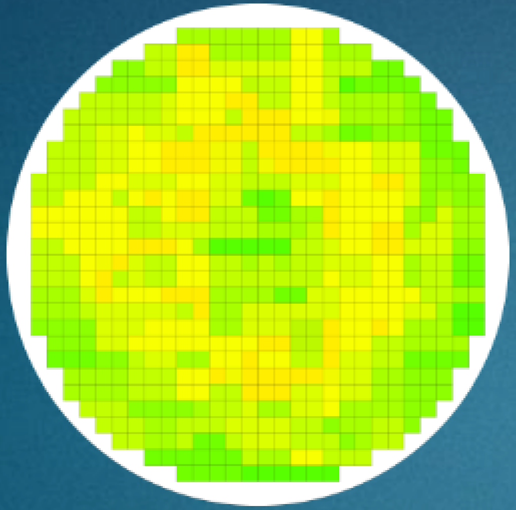

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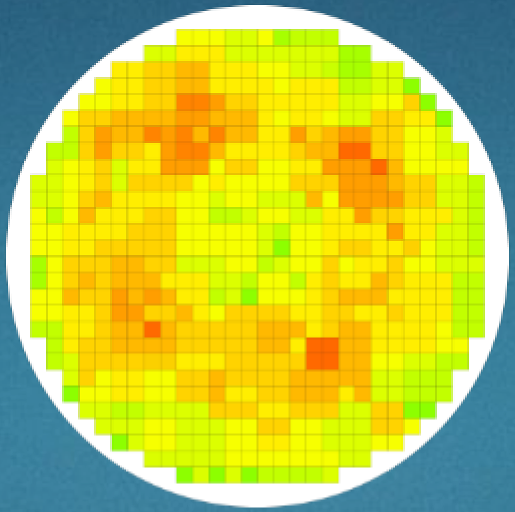

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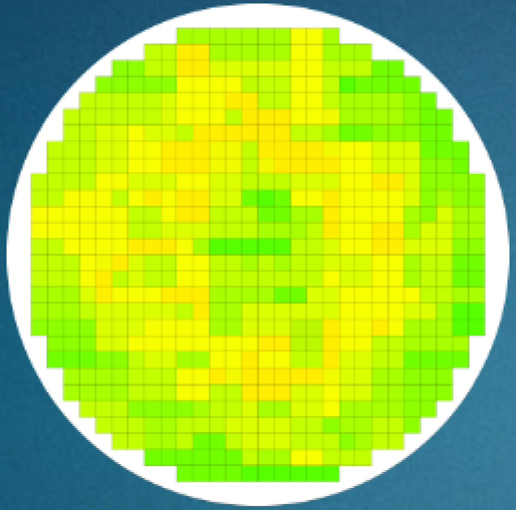

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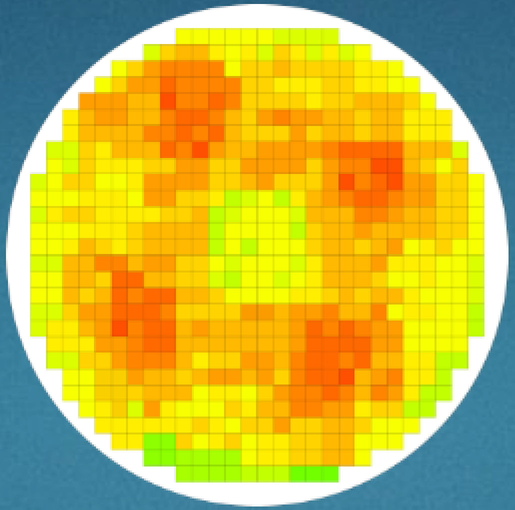

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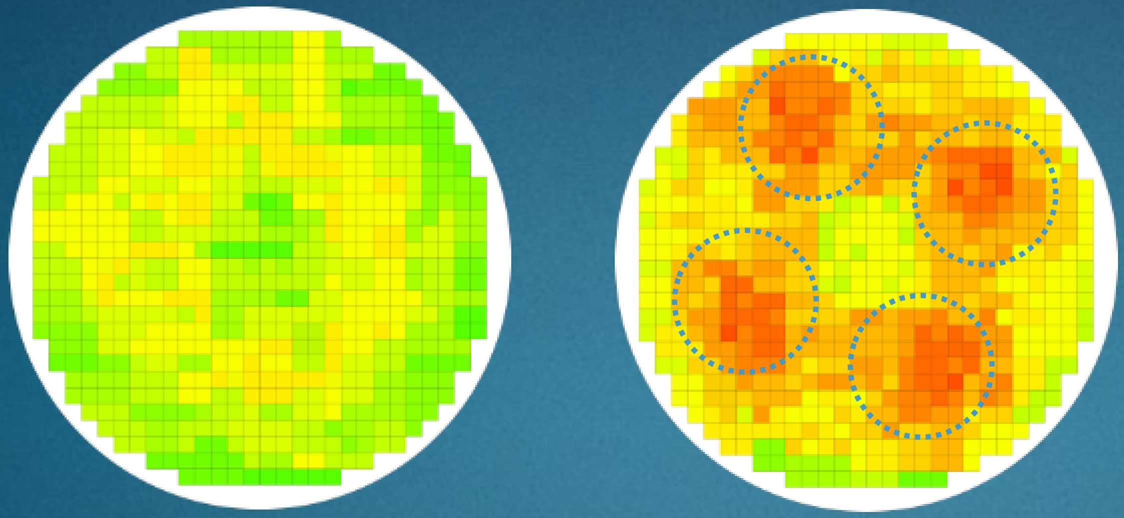


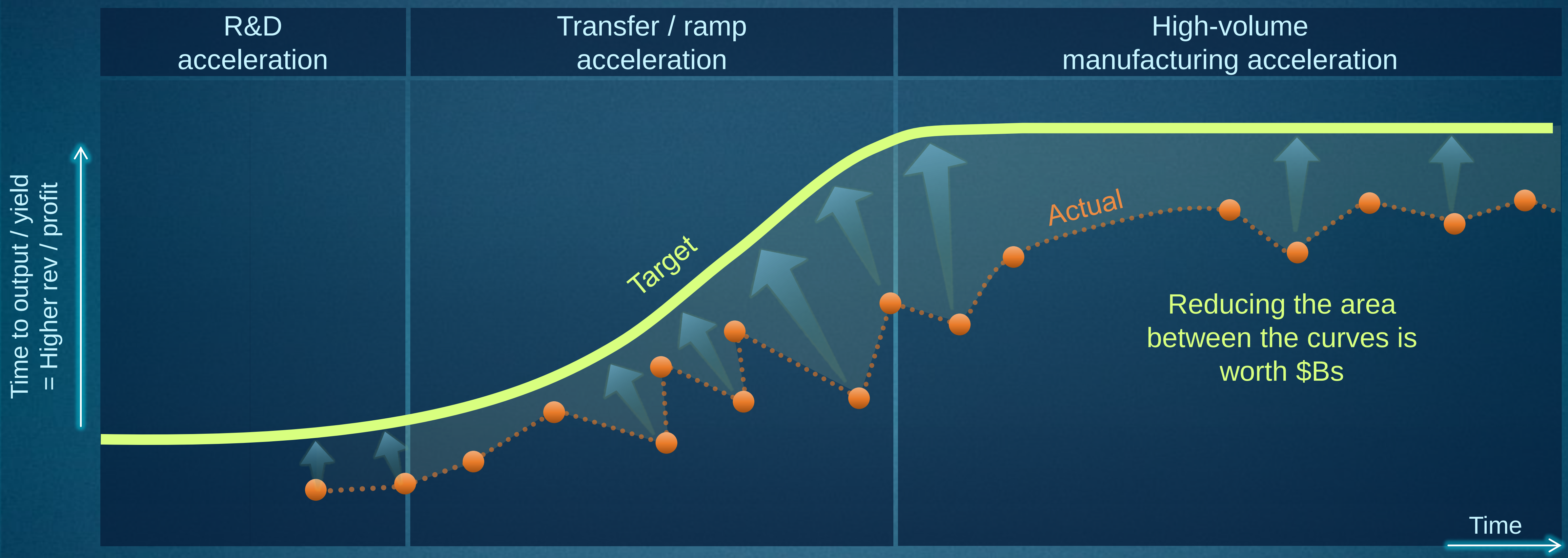
Sparse sampling

Massive sampling reveals process signature

Process signature helps identify process issue

Shortens time to root cause from days to minutes

The Value of Time-to-Market



Shorter Time-to-Market is worth $billions to customers and the technology ecosystem

Source: Applied Materials

Applied Materials Israel Main Tasks in MADEin4

- **Optical wafer inspection**
  - Improve optical wafer inspection sensitivity to keep up with the shrinking size of killer defects and provide new information, while improving throughput and productivity – new optics, high-performance computing and system design

- **Ebeam wafer inspection**
  - Improve ebeam wafer inspection sensitivity to keep up with the shrinking size of killer defects and provide new information and expand the application space, while improving throughput for massive across-wafer scanning – new column, modules and system design

Sensitivity | **Productivity** | **New information**

APPLIED MATERIALS

Applied's Main Collaborations in MADEin4

Advanced Wafers

Brightfield image processing / data handling

Stage and positioning

Brightfield optical inspection

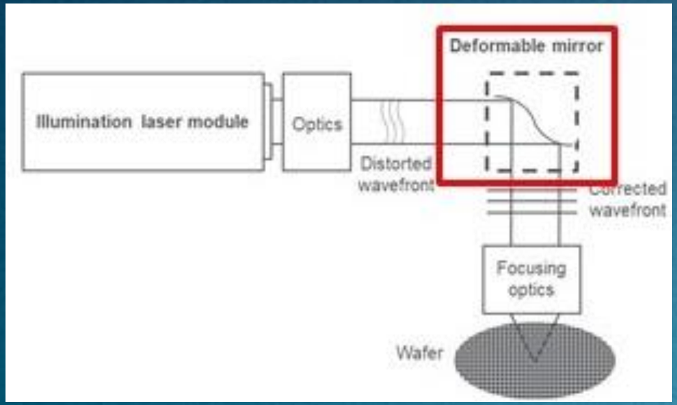
ICT

New / improved metrology through cross-tools Machine Learning analysis

Ebeam inspection and metrology

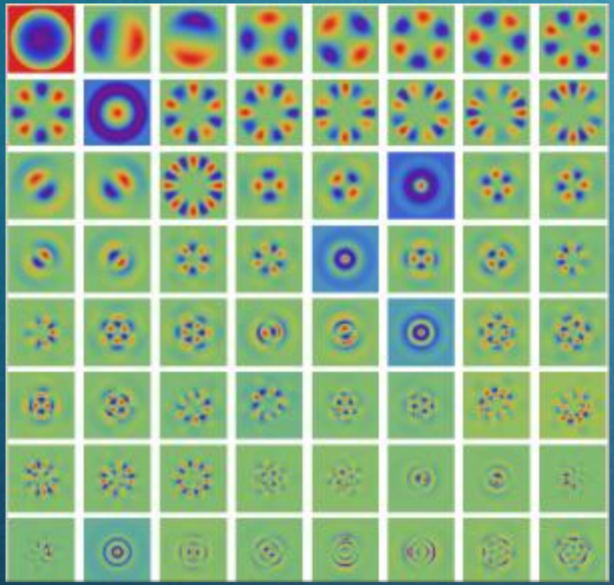
Optical Wafer Inspection – Adaptive Wavefront Control

Higher sensitivity and matching

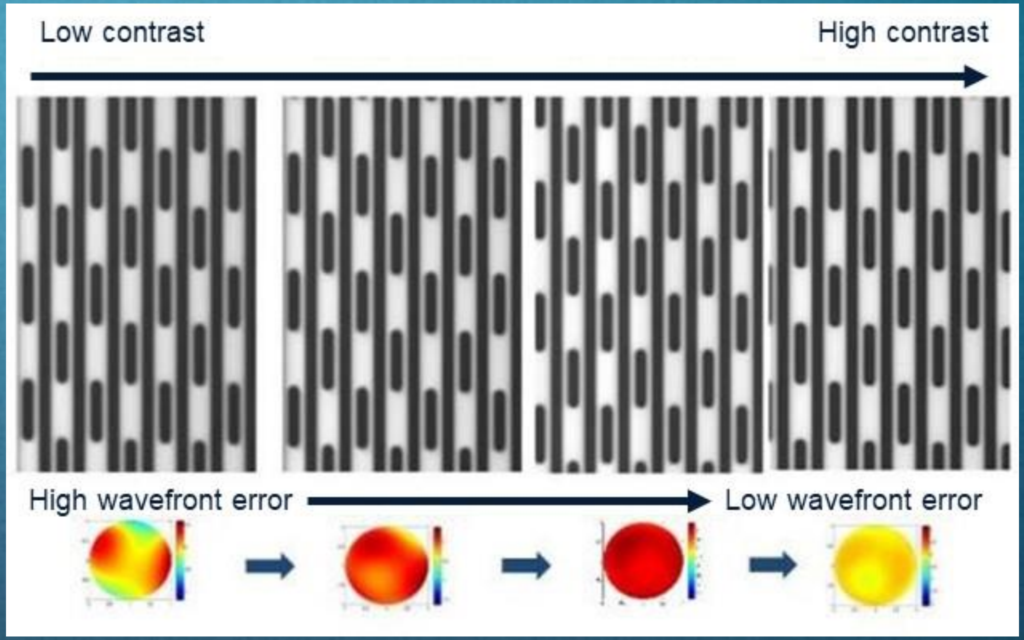


Adaptive scheme

Adaptive mirror prototype



Wavefront control

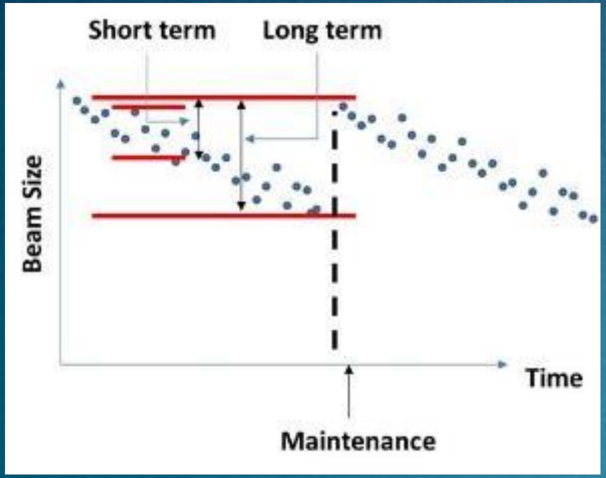


On-tool optical imaging

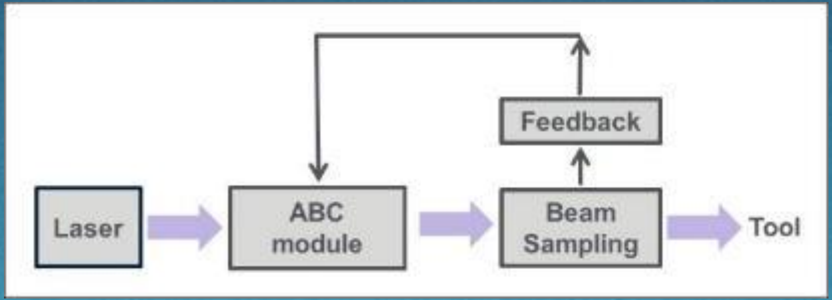
Source: OKO, Applied Materials

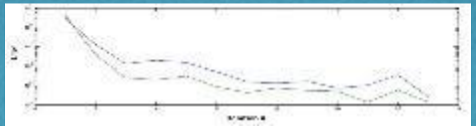
Optical Wafer Inspection – Automatic Laser Beam Parameters Control

Higher sensitivity, repeatability, stability productivity and matching

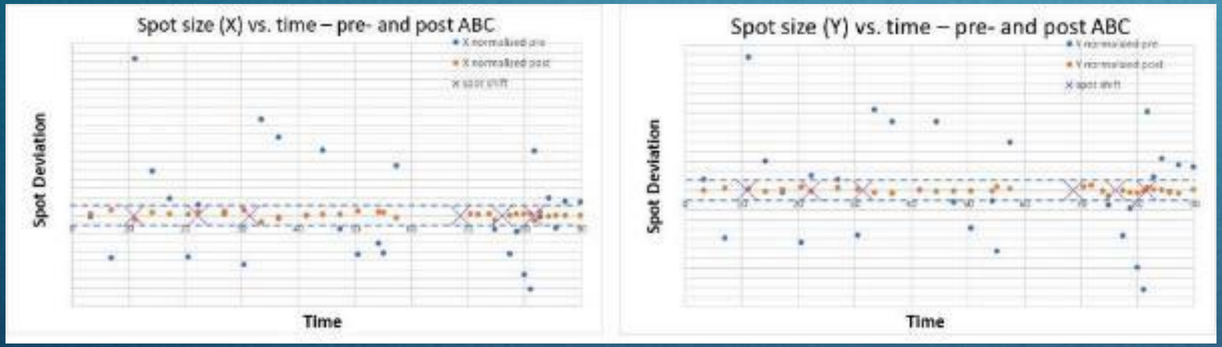


Motivation

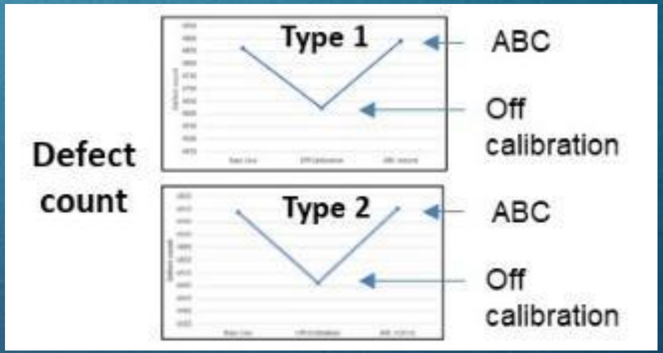




Adaptive scheme and convergence



On-tool performance

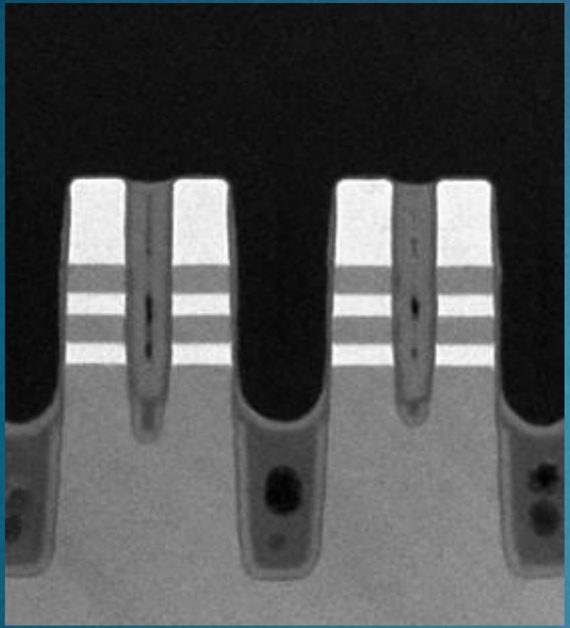


On-tool performance

Source: Applied Materials

Optical Wafer Inspection – Flexible Optics Modes

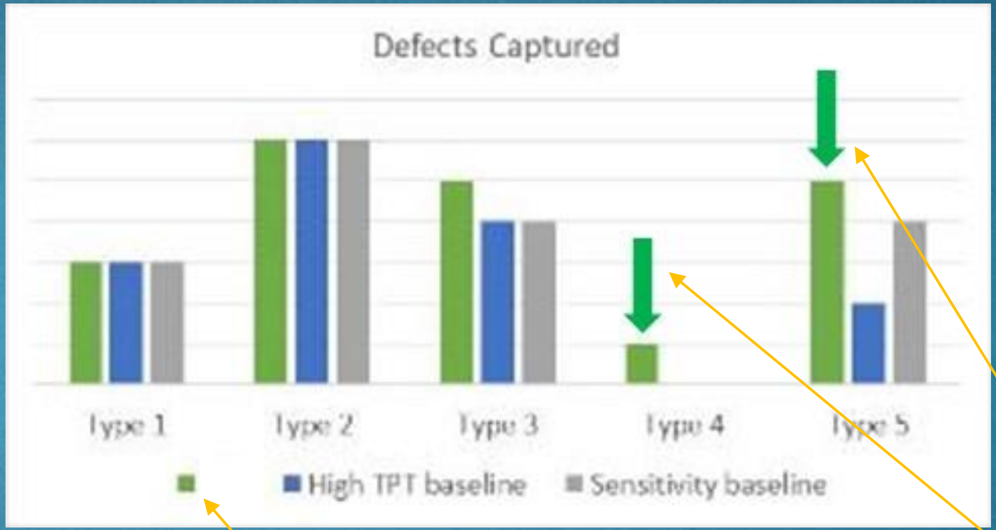
Higher sensitivity and productivity



Source: imec

Tests performed on the imec Mont Blanc wafer, with advanced forksheet device designs

Overall similar or higher sensitivity and higher throughput on all analyzed defect types



New mode

Higher sensitivity & throughput

Higher sensitivity

Source: Applied Materials

Optical Wafer Inspection – High Performance Computing System

Higher productivity and flexibility

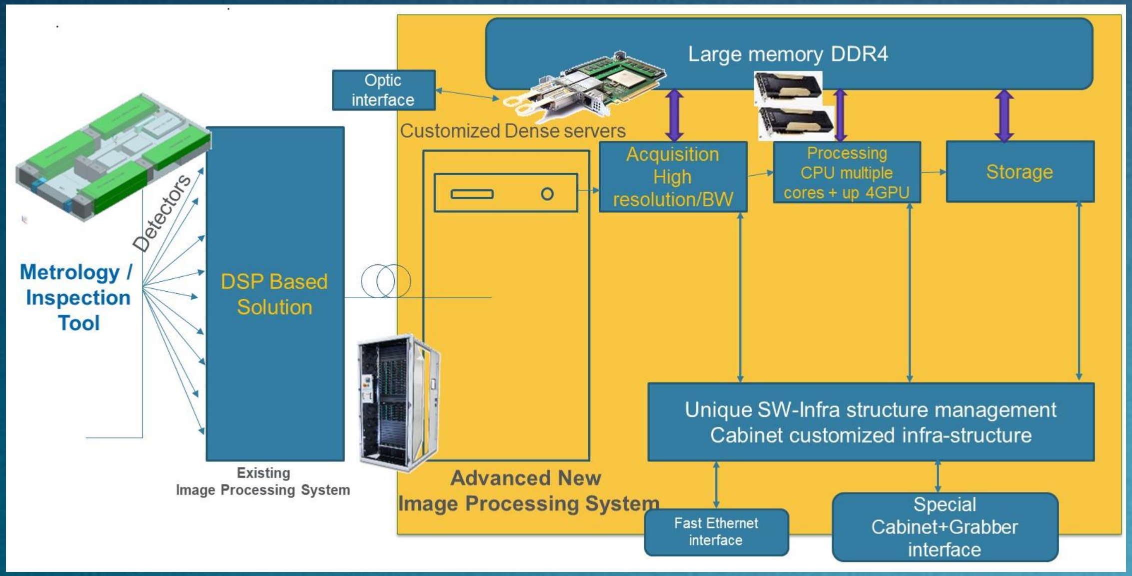
PRODRIVE TECHNOLOGIES

- Main challenges
  - Wafer image acquisition: high data rate data acquisition channel, with incoming data rate of ~10’s of GB/s
  - Execution of parallel computer vision algorithms and advanced deep learning algorithms
  - Massive real-time processing power to support complex algorithms
  - Massive data communication with advanced periphery systems
  - Huge storage volume
  - Scalable architecture to support future algorithms and computing technology – HW and SW
  - Environmental:
    - Power consumption and heat dissipation limitations, high reliability requirements
    - Fab noise restrictions and limitations
    - Computing system cabinets footprint limitations
  - Highly efficient cost/performance computing

High Performance Computing System

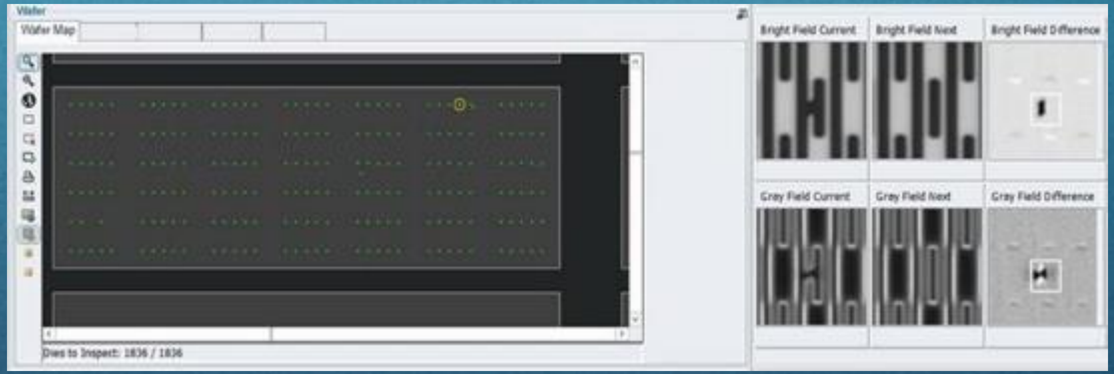
- **Development methodology**
  - Use of off-the-shelf core components (HW and SW, including open source) to accelerate development time
- The system development required optimization of:
  - HW and SW architecture
  - Processing dispatching
  - Load balancing
- Solutions include
  - Use of a tailored server architecture for the specific Use-case
  - Use of accelerator/GPU for the specific Use-case
  - Design of data acquisition path from the detectors with off-the-shelf components

High Performance Computing System



High performance computing architecture

High data rate data grab module developed by PRODRIVE

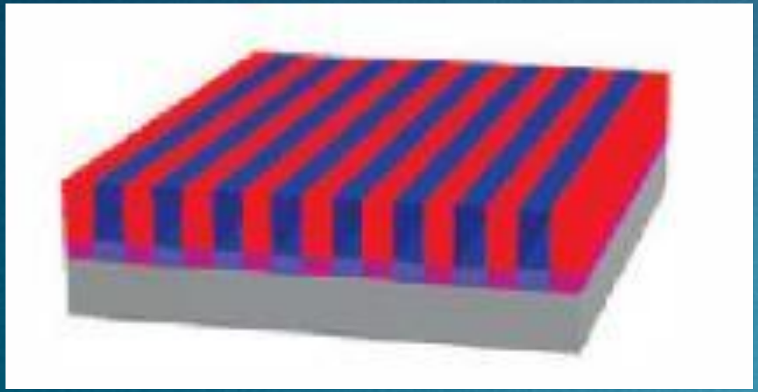


End-to-end defects detection on programmed wafer

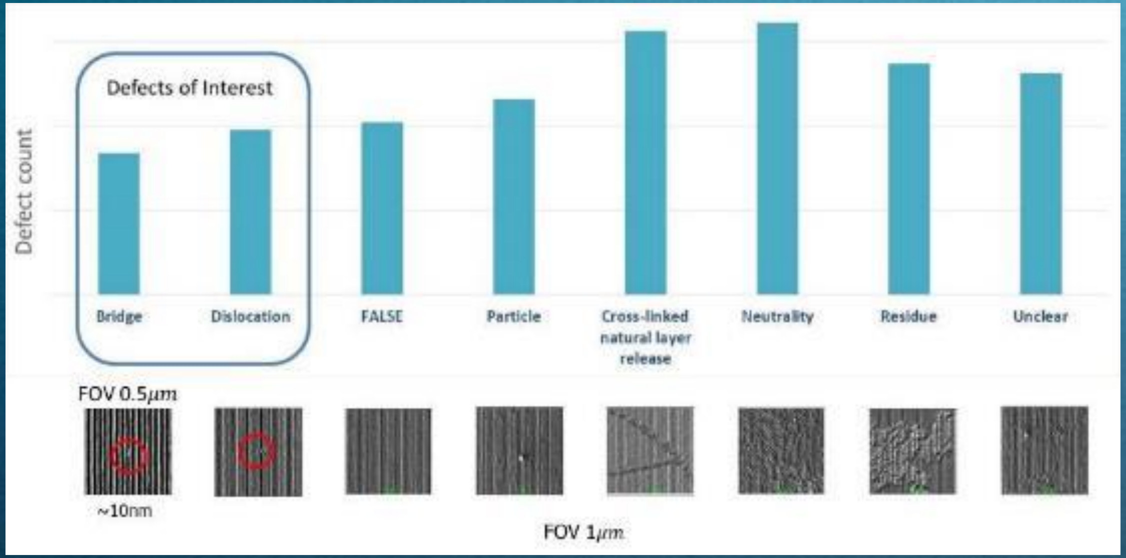
Source: PRODRIVE, Applied Materials

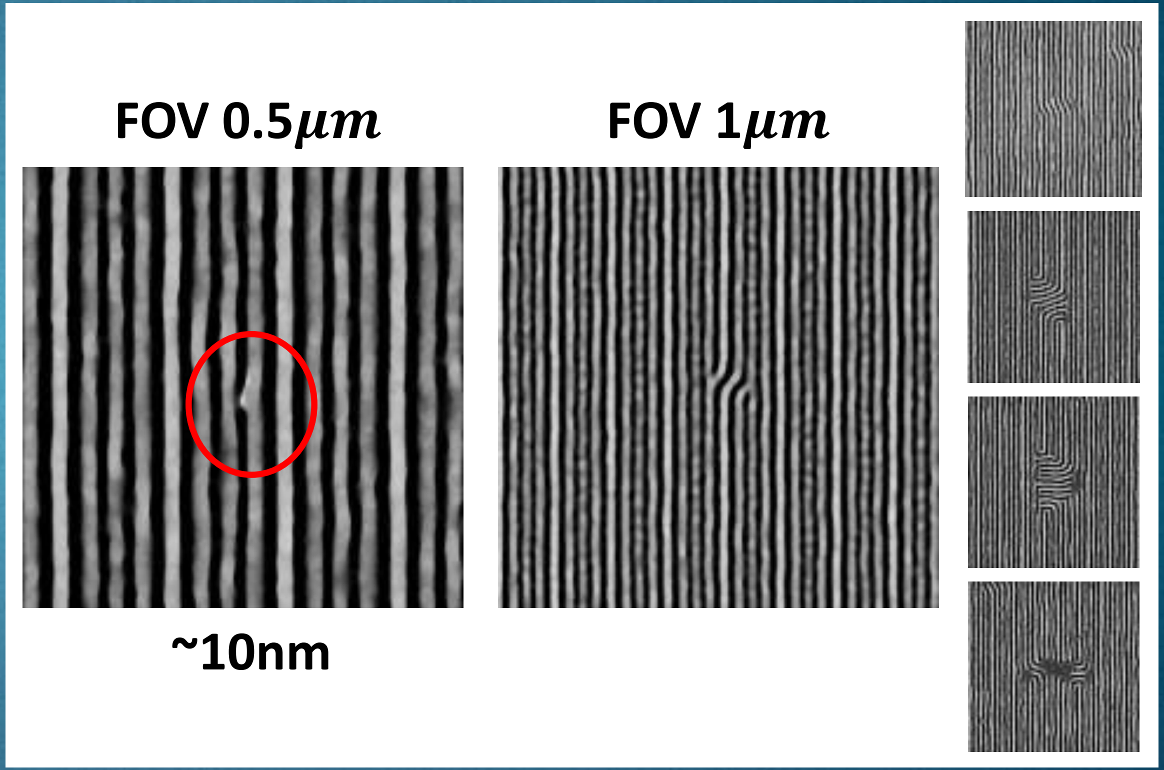
LETI DSA Wafer – Optical Wafer Inspection

Objectives: detect DSA process related defects, with focus on small defects



Source: LETI



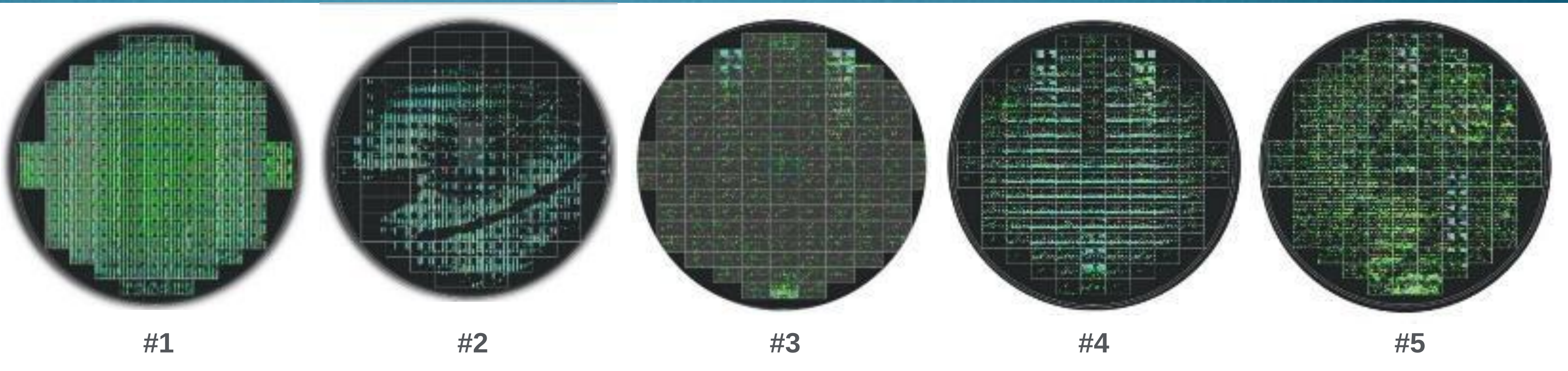


Source: Applied Materials

New Metrology Information – Across-tools ML Analysis

Objectives: provide massive raw data to validate a Machine Learning algorithm developed by MADEin4 partner (Mentor Graphics) to provide new metrology information through analysis of data acquired by various inspection and metrology tools

#	Layer Name
1	Metallization M2
2	Metallization M1
3	litho M1
4	etch M1
5	litho M2
6	etch M2
7	litho V1
8	etch DD V1
9	litho V1
10	etch DD V1



Defect maps

A set of imec wafers was used for collecting raw inspection and metrology data using various metrology techniques developed by MADEin4 partners

Source: Applied Materials

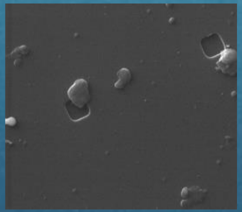
Ebeam Wafer Inspection
Higher sensitivity and productivity

New column by ICT

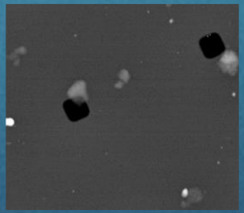
- New key modules include new column developed by ICT, with new electron emitter and improved detectors
- System developments including electronics and controls, motion control, algorithms and new enclosure
- Higher throughput and better imaging was enabled by the new column and by the improved detection
- Expanded application space enabled by the new development

A new detector was developed for improved performance, enabling

- New imaging information to be extracted from the target
- Higher throughput at new working points



Baseline imaging



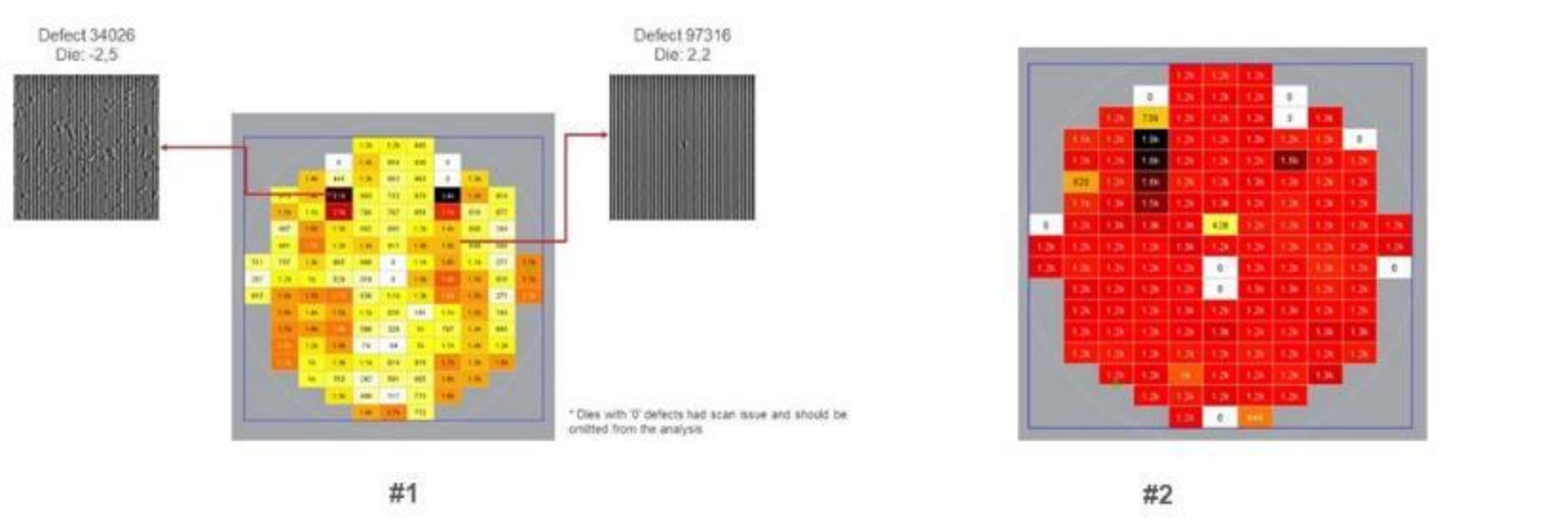
Improved imaging

Source: ICT, Applied Materials

New Metrology Information – Across-tools ML Analysis

Objectives: provide data to validate a Machine Learning algorithm developed by MADEin4 partner (Mentor Graphics) to provide new metrology information through analysis of data acquired by various inspection and metrology tools from same wafers

Layer Name
litho M1
etch M1



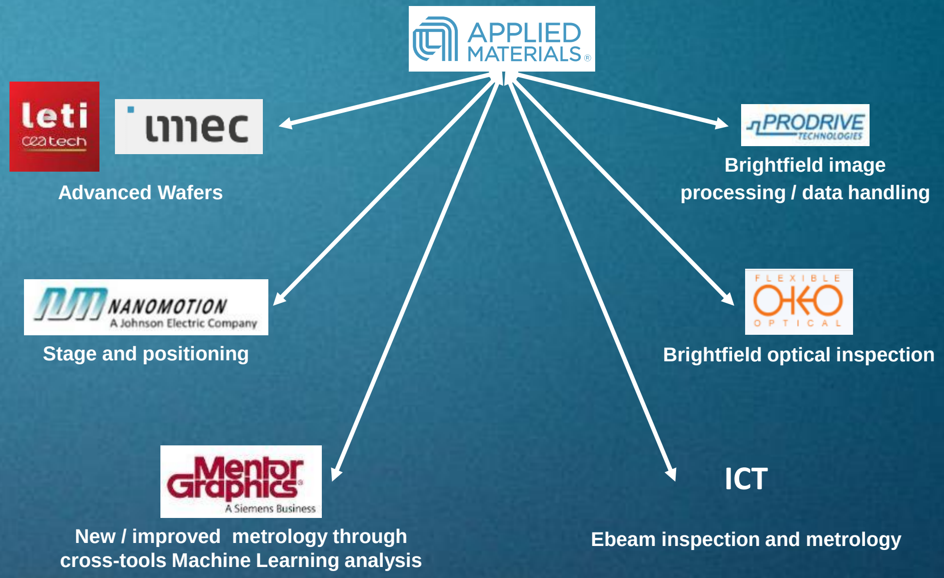
Cross wafers ebeam inspection defect density maps

A set of imec wafers were used for collecting raw inspection and metrology data several metrology techniques developed by several partners

Source: Applied Materials

Summary

- Applied Materials Israel developed, as part of MADEin4, optical and ebeam wafer inspection platforms to address the metrology and inspection challenges of advanced semiconductor manufacturing: higher sensitivity, higher productivity and new metrology information
- Sensitivity productivity and new metrology information developments were made possible through multiple module-level developments as well as system-level designs
- Sensitivity and productivity were demonstrated on advanced wafers
- Developments were made through collaboration with multiple MADEin4 partners



MADEin4 ECSEL JU רשות החדשנות Israel Innovation Authority APPLIED MATERIALS® make possible

MADEin4

Thank You For Your Attention

Acknowledgements

ECSEL Joint Undertaking
Electronic Components and Systems for European Leadership

MADEin4

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826589. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, Italy, Austria, Hungary, Romania, Sweden and Israel

Thank you, all Applied Materials Israel colleagues, and all MADEin4 partners

Thermo Fisher SCIENTIFIC

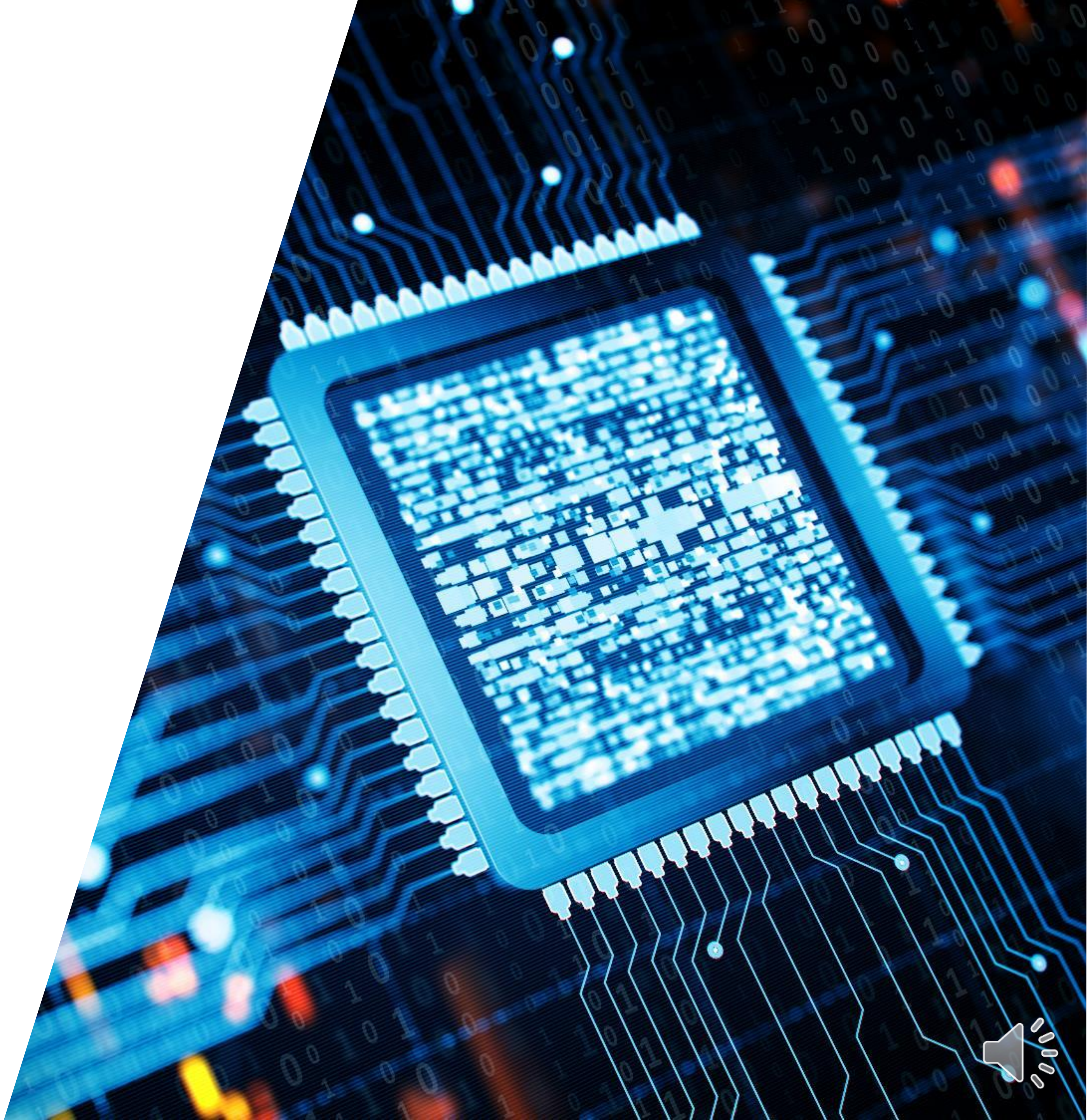
Metrology and characterization innovations meeting the new Industry 4.0 challenges in the semiconductor industry

Dr. A. Frank de Jong

Director strategic programs
Materials and Structural Analysis Division

SEMI-EU Webinar, September 15, 2022

The world leader in serving science



Agenda for this presentation

1. Key challenges and objectives for metrology

2. Metrology platform improvements

Several examples

3. Metrology platforms for Industry 4

4. Conclusions

1. Key challenges and objectives for Metrology Platform developments in MADEin4

Main challenge:
Higher complexity
***And* Higher productivity**

(3D) complexity

… *AND* productivity

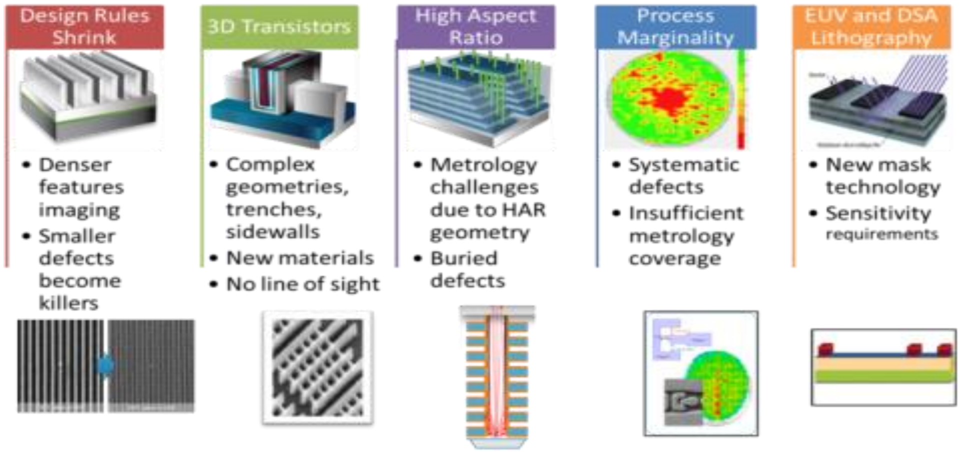
Key objectives:

Develop and qualify new platforms

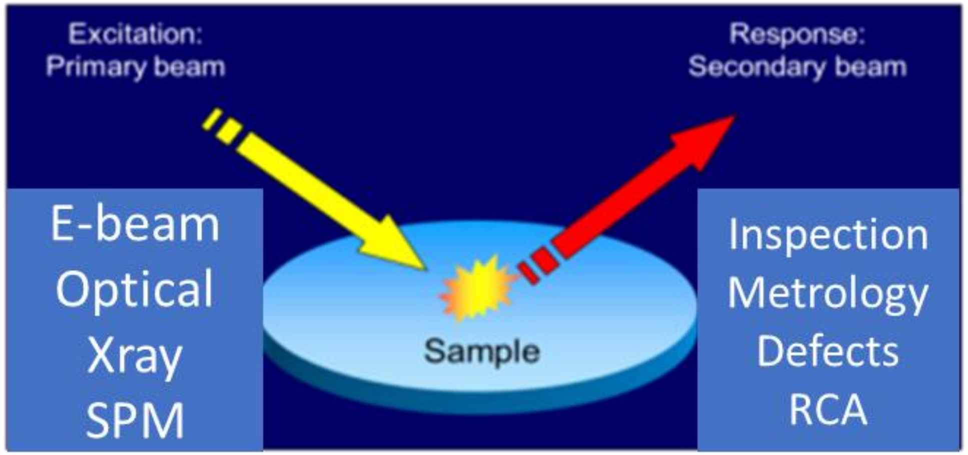
- High-productivity metrology and inspection tools for semiconductor and automotive industry **(Booster 1)**
- Ready for "industry 4" CPS:
  - Higher data rates (acquisition, processing)
  - Providing link for smart use of data to improve the over-all productivity

(Booster 2)

2. MADEin4 metrology platform improvements



Metrology challenges by more complex chip production



Throughput challenge at higher resolution: *smaller interaction volume, less signal*

Examples:
- Faster wafer inspection & metrology by Ebeam and BF *(previous presentation)*
- Multi-channel integrated OCD metrology
- Faster Scanning Probe Metrology tool
- Faster TEM analysis workflow

Higher tool productivity (Booster 1):
- Better sources
- Better detectors
- New modalities
- Improved sample handling
- Enhanced automation
- Smaller (sw) overheads

2. Metrology platform improvements (example 1)

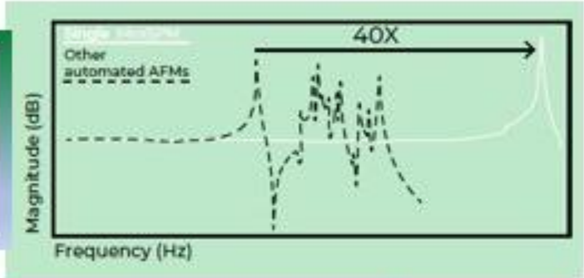
MADEin4

2. Metrology platform improvements (example 2)

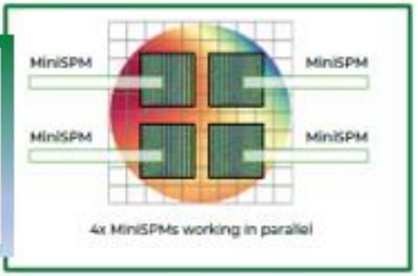
NEARFIELD INSTRUMENTS Surface Metrology: QUADRA

Offers High Througput

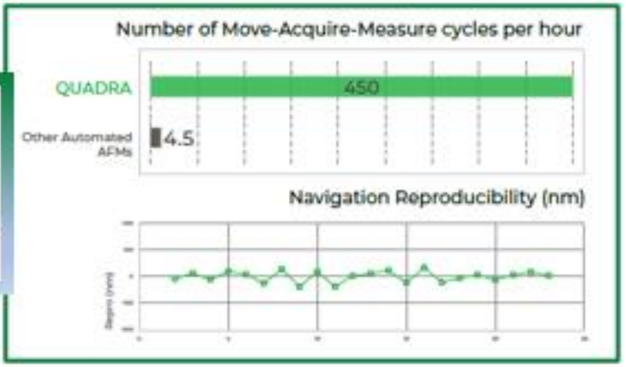
Very high bandwidth of each Miniaturized SPM (40x higher than existing automated systems)



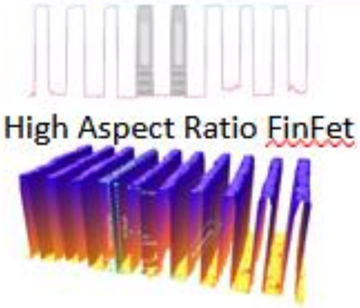
QUADRA: 4x Mini-SPMs operating in parallel



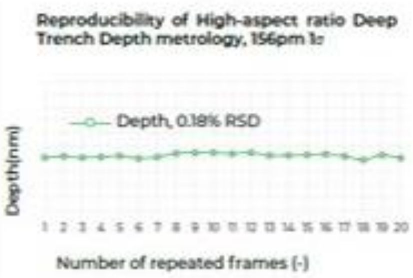
Very high MAM, while maintaining imaging performance



Offers Value Metrology



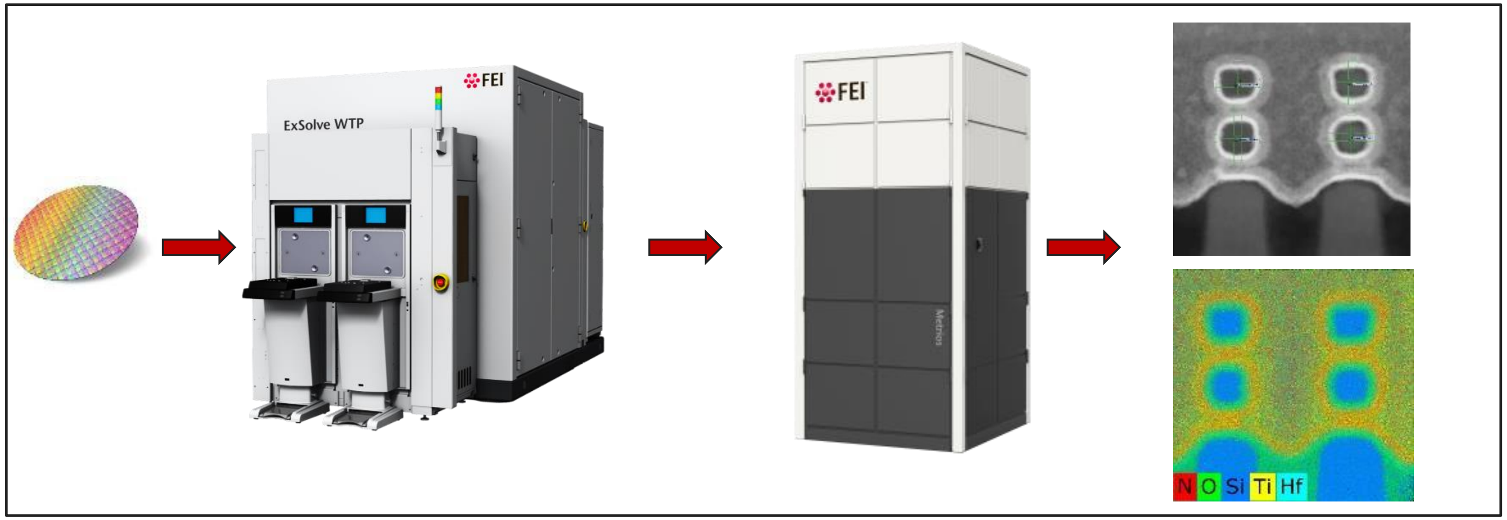
High Aspect Ratio FinFet



MADEin4

2. Metrology platform improvements (example 3):

TEM Workflow for fast HV local atomic-scale metrology

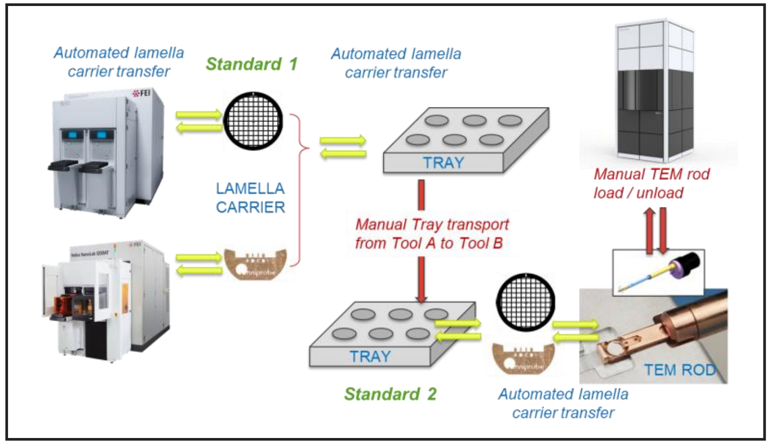


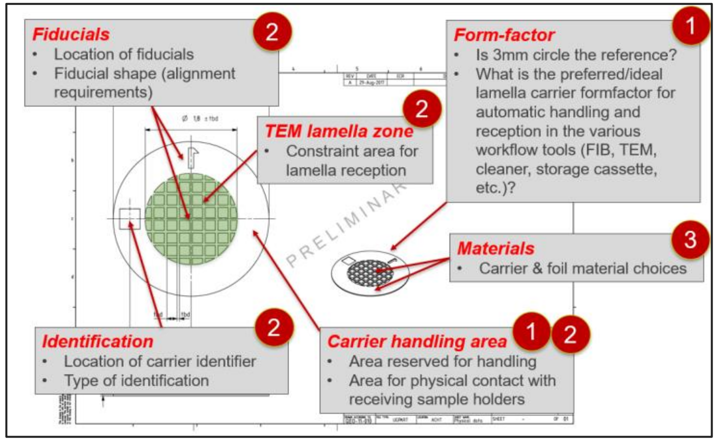
TEM workflow:

- Preparing tiny lamella from a wafer
- Analyzing cross-sections in TEM
- Sample handling challenges
- Standarization

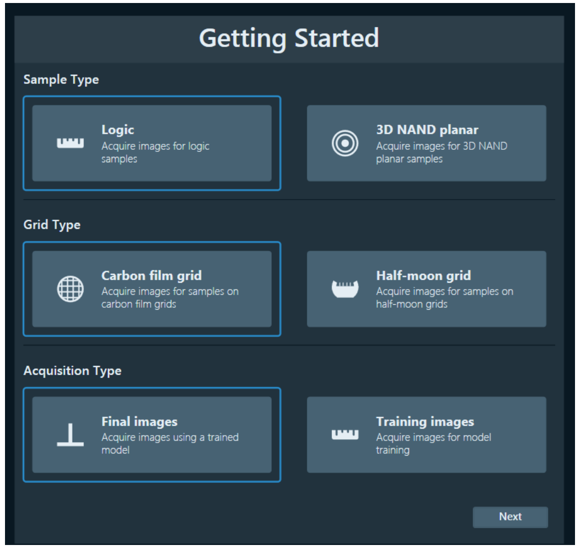
Automation challenges:

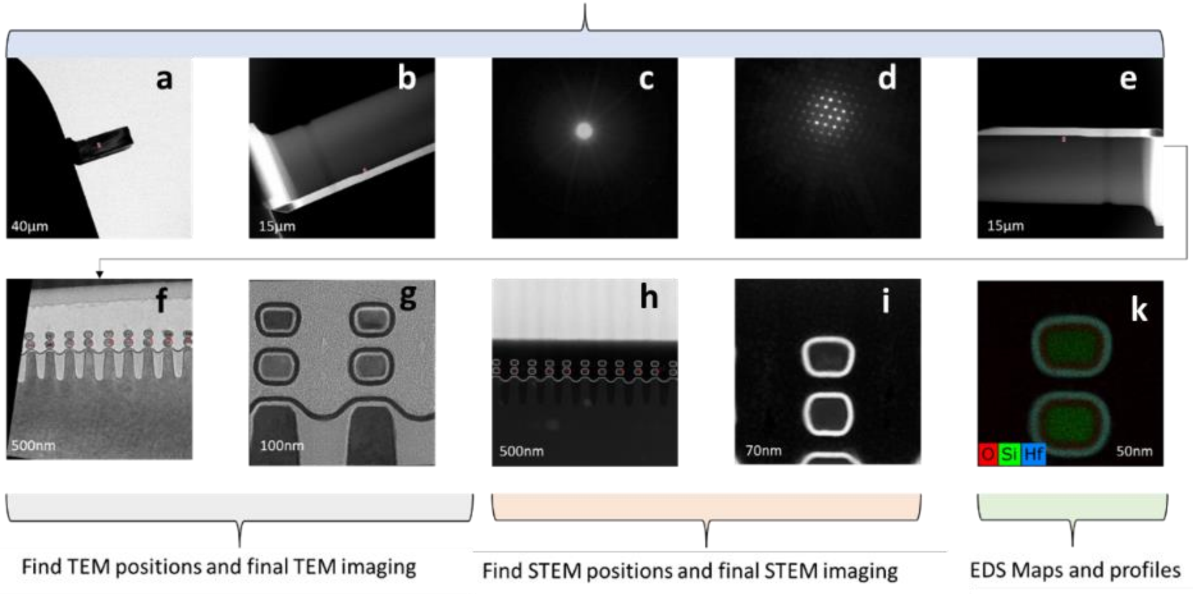
- Different questions / samples
- Many TEM modes
  - *TEM imaging, STEM imaging, metrology, inspection, EDX compositional analysis*
- Retaining flexibility for customer

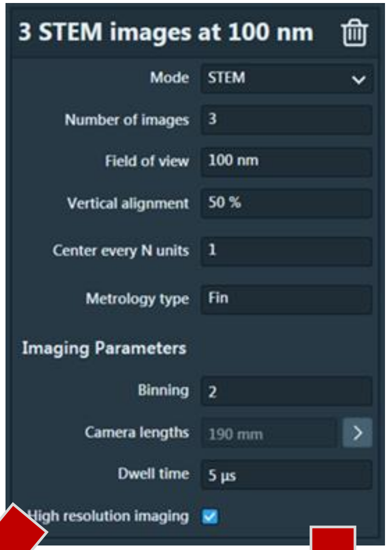




2. (example 3): *TEM workflow Smart Automation*



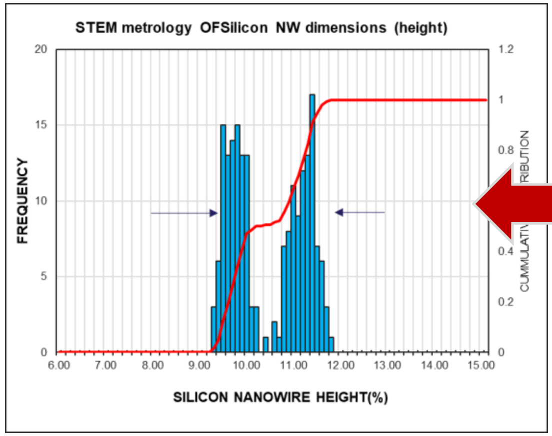


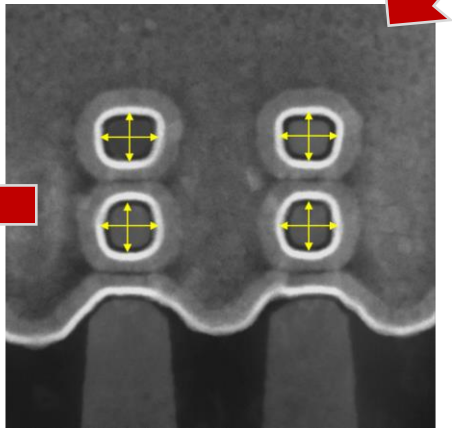


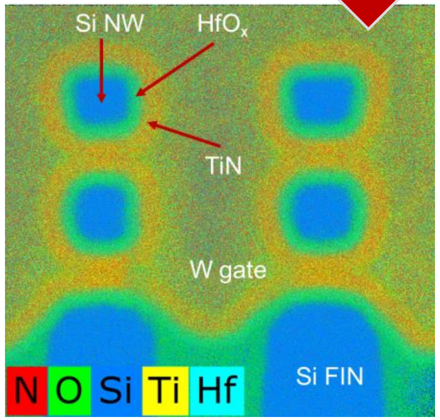
- **Automated set-up** of experiments

  Powered by Machine Learning
- **Automated acquisition**

  TEM / STEM / EDS
- Targeted use cases: logic, DRAM, 3D NAND







3. Metrology platforms for Industry 4.0

Metrology platforms as Cyber Physical Systems

Industrial maturity in Industry 4.0 according the Acatech standard

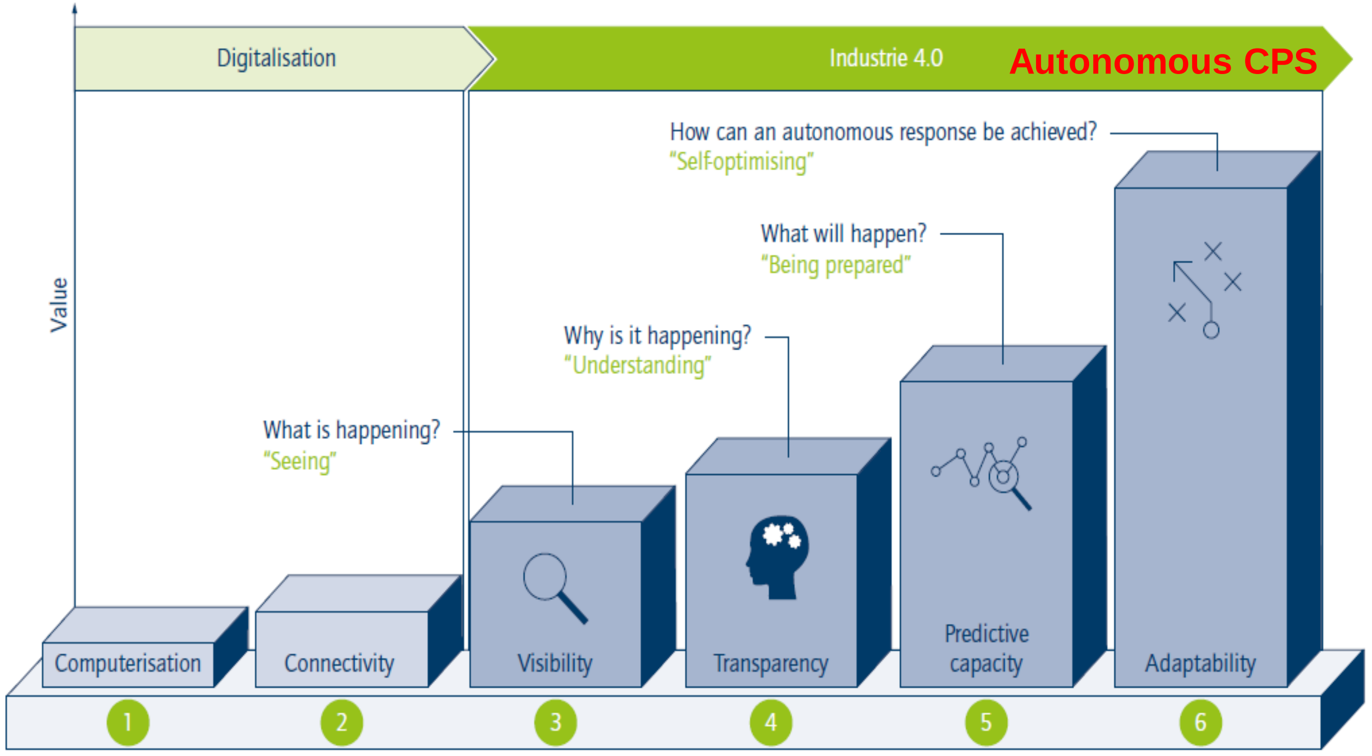


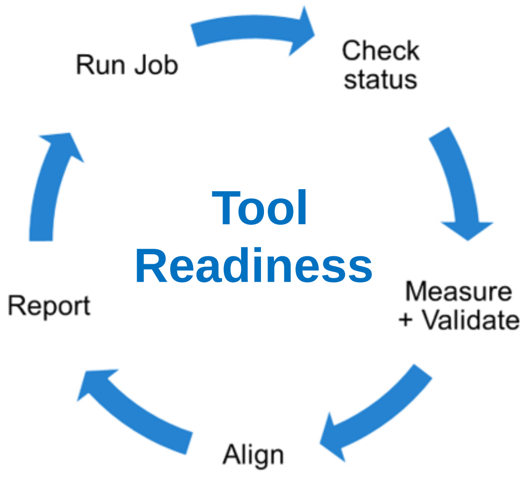
Figure 5: Stages in the Industrie 4.0 development path (source: FIR e. V. at RWTH Aachen University)

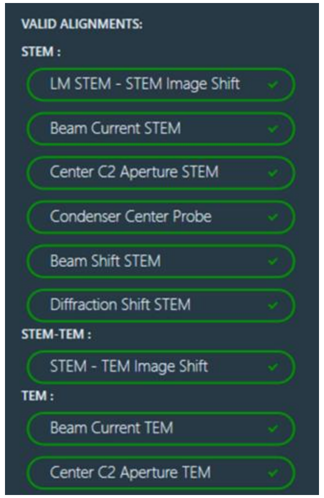
Enhancing productivity by making tools smart; ready for Industry 4.0 (Booster 2)

- 2 Connectivity
- 2 Quality monitor
- 3 Smart acquisition
- 4 Smart tool set-up
- 5 Predictive tool availability
- 6 Adaptive tool readiness

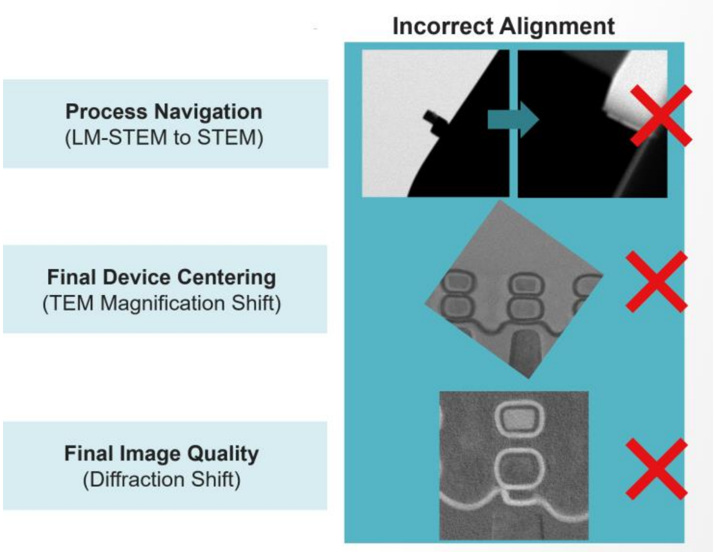
3. Tool Readiness

- Enables high quality data and automation robustness
- Maintains 18 critical tool alignments on a daily or weekly basis
- Automated alignments reduce dependency on operator skill

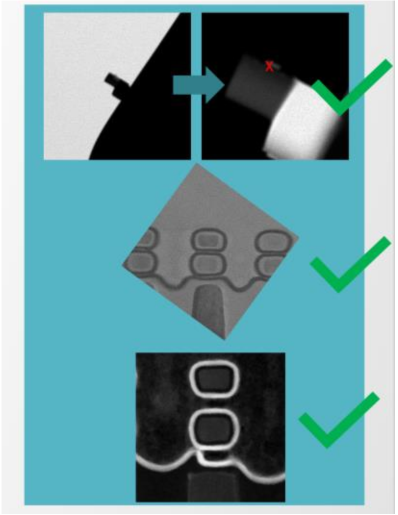




Tool readiness alignment check



Alignment needed

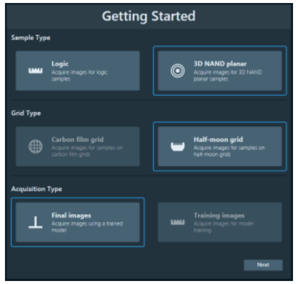


Alignment complete

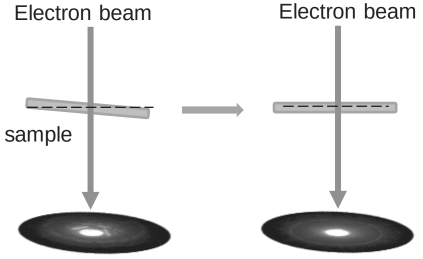
Automated S/TEM Metrology workflow

Automated S/TEM

- 4th gen automatic S/TEM
- Smart Automation powered by ML
- Smart Align Feature powered by ML



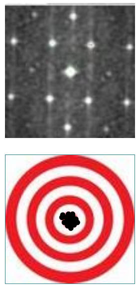
Smart Automation



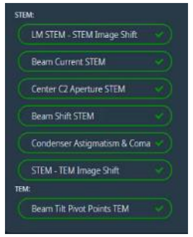
Smart Alignment

Consistent data

- <0.75% metrology accuracy
- Tool readiness
- Image quality monitoring



Mag calibration



Tool readiness

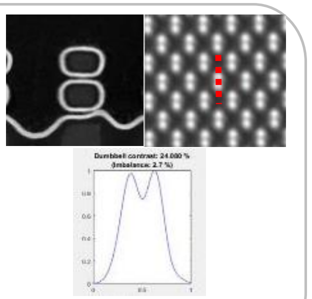
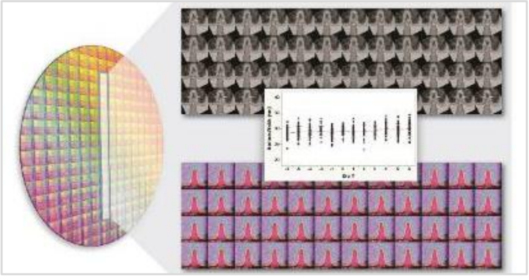


Image quality metrics

High volume S/TEM reference data

- High volume TEM data
- Connected workflows
- Statistically relevant S/TEM reference data

Workflow



High volume TEM reference data

4. Conclusions on metrology platform developments

1. Enhance productivity AND address higher complexity

2. Significant metrology platform improvements reached in MADEin4 project

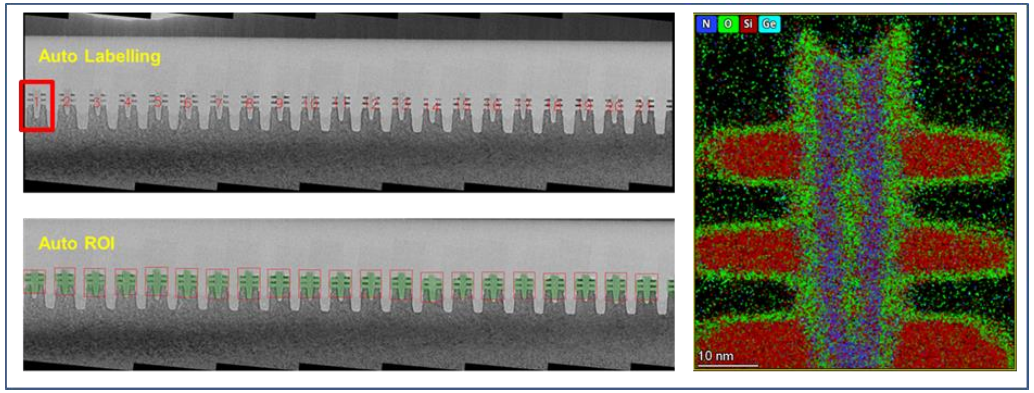
Examples:

- **in-line integrated multi-channel OCD yields extra info and faster**
- **multi-head SPM improves speed 100x**
- **automated TEM metrology yields atomic-scale HV data quickly**

3. Metrology platform as CPS is ready to be part of Industry 4.0 Data driven FAB

Metrology and characterization innovations meeting the new Industry 4.0 challenges in the semiconductor industry

Thank you for your attention



Acknowledgements:
- inputs from NOVA and NFI
- MADEin4 coordinator, SEMI-EU
- Thermo Fisher colleagues

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826589. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, Italy, Austria, Hungary, Romania, Sweden and Israel

Practical Machine Learning Applications for Semiconductor Manufacturing.

Andres Torres,
Siemens EDA

September 15th 2022

Outline

Differences between Machine Learning for Social Media and Semiconductor Manufacturing

Leveraging ML models across multiple applications

- Single Process Monitoring
- Multiple Process Sequence
- Preventive Maintenance

Differences between Machine Learning for Social Media and Semiconductor Manufacturing

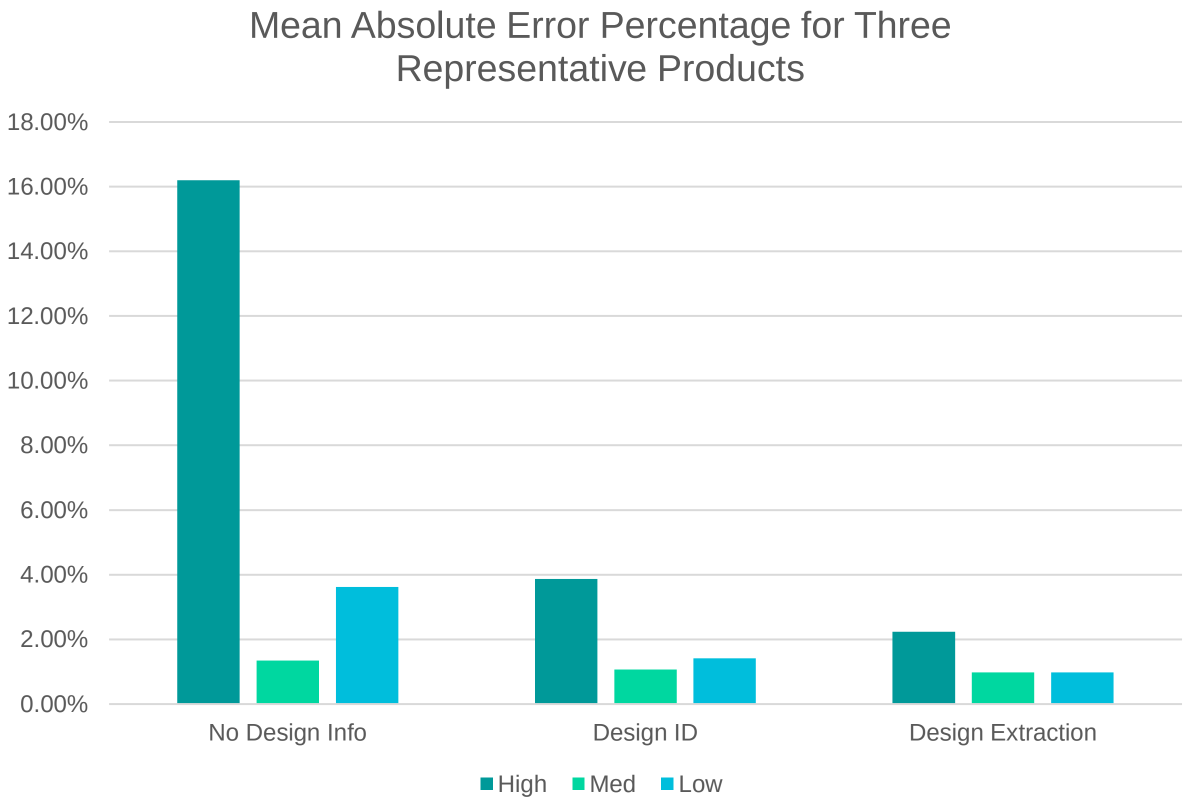
Social Media

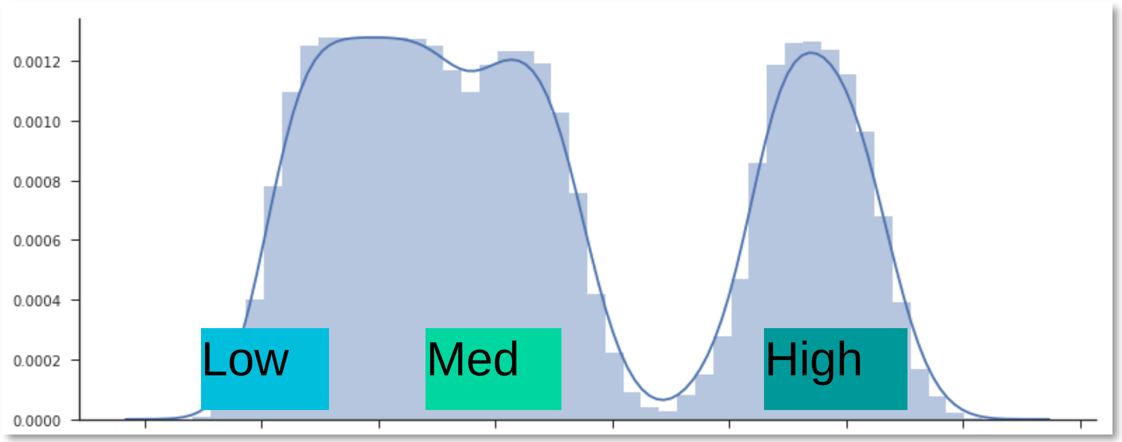
Number of measurements per user **10^2**
Number of users per month **10^7**
Human Behavioral based
Leads to narrow and deep data matrices

Semiconductor

Number of measurements per wafer **10^3**
Wafers per month **10^5**
Physics based
Leads to wide and shallow data matrices

Single Process Example: Chemical Vapor Deposition process
Quantifying the benefit of incorporating design features (Stefan Schueler et al)





The more it is known about the interactions of different products with the process, the better the equipment (in this case a CVD tool) can be better characterized, enabling virtual metrology to be performed not only for previously observed products but for new products as well.

Stefan Schueler, C. H. (2021). Virtual metrology: how to build the bridge between the different data sources. *Proceedings Volume 11611, Metrology, Inspection, and Process Control for Semiconductor Manufacturing.* SPIE.

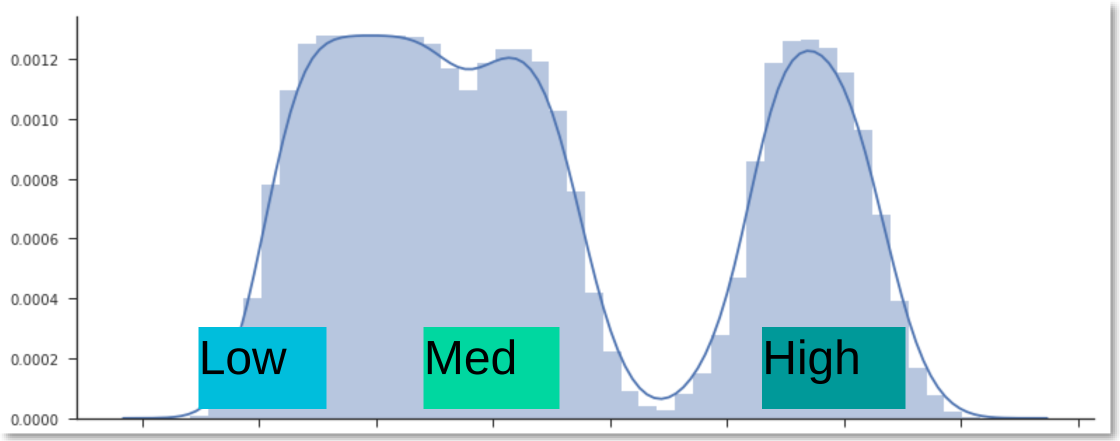
Single Process Example: Chemical Vapor Deposition process

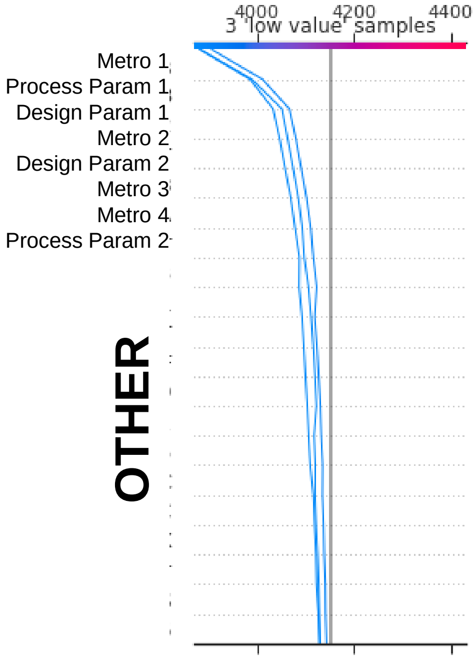
Identifying root causes of abnormal conditions

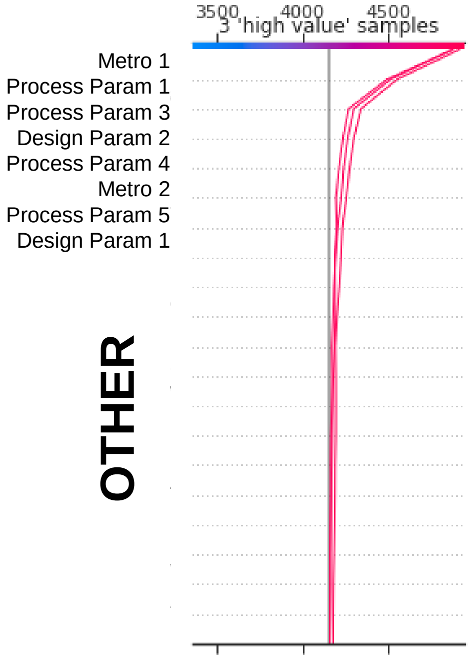
Machine Learning techniques like SHAPley analysis permit the determination of the main contributors to abnormal conditions when members of the tails of the distribution are analyzed.

The effects leading to low or high conditions are not necessarily the same between populations.

This knowledge can serve to assist Automatic Process Control systems during manufacture.

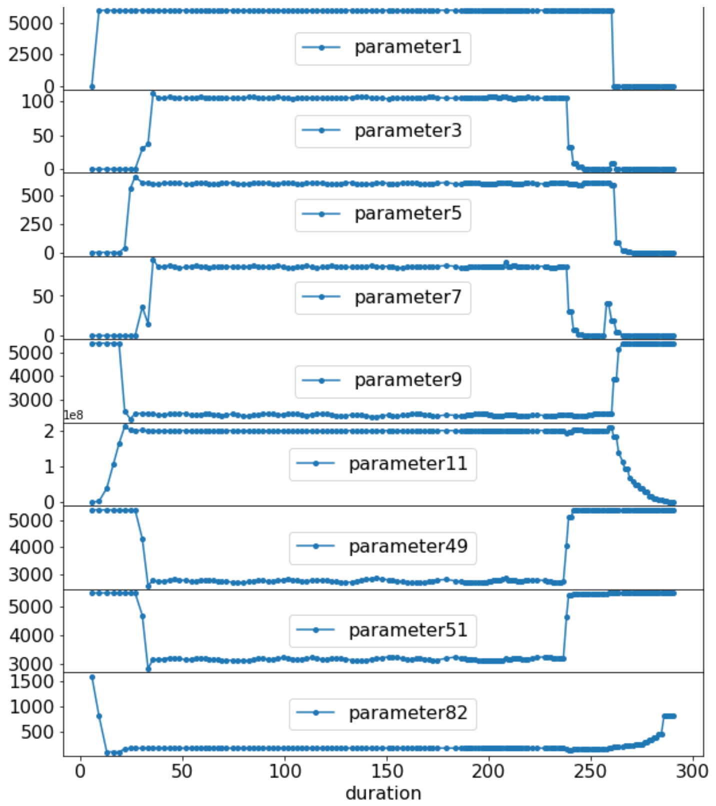




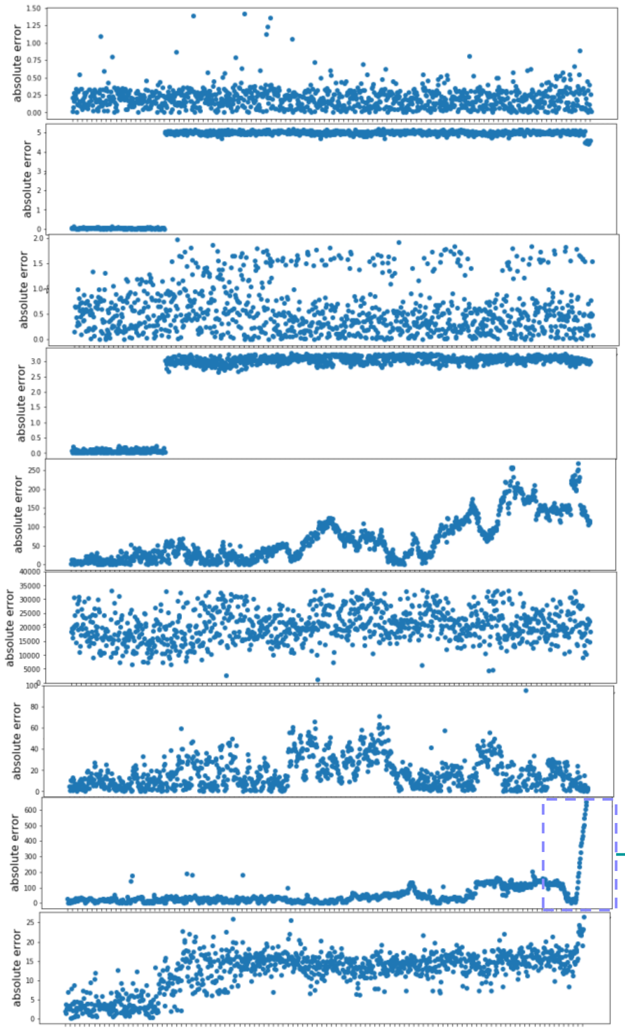


Feature Engineering for Preventive Maintenance (electro plating tool)

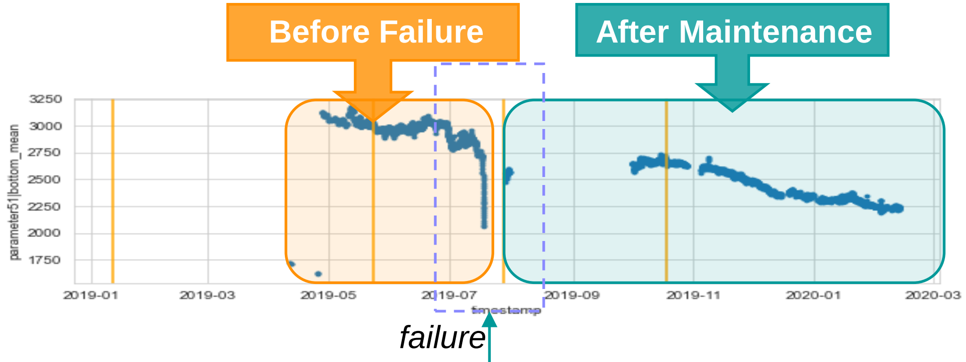
Raw input data



Feature engineering to create state features



Test



Analysis of multiple signals are analyzed to determine possible failure conditions.

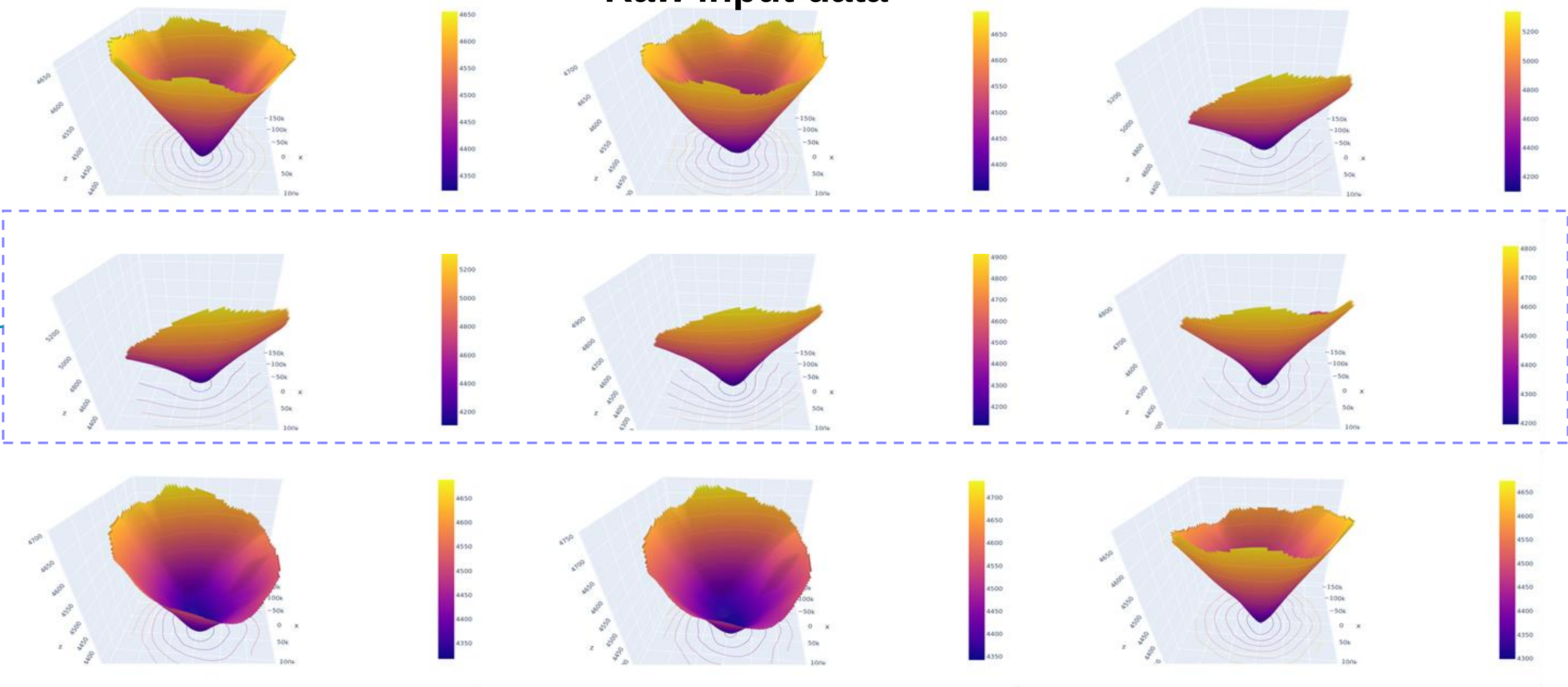
In the simplest case, one variable can explain the observed behavior

Feature Engineering for Preventive Maintenance (Chemical Vapor Deposition Tool)

Feature engineering

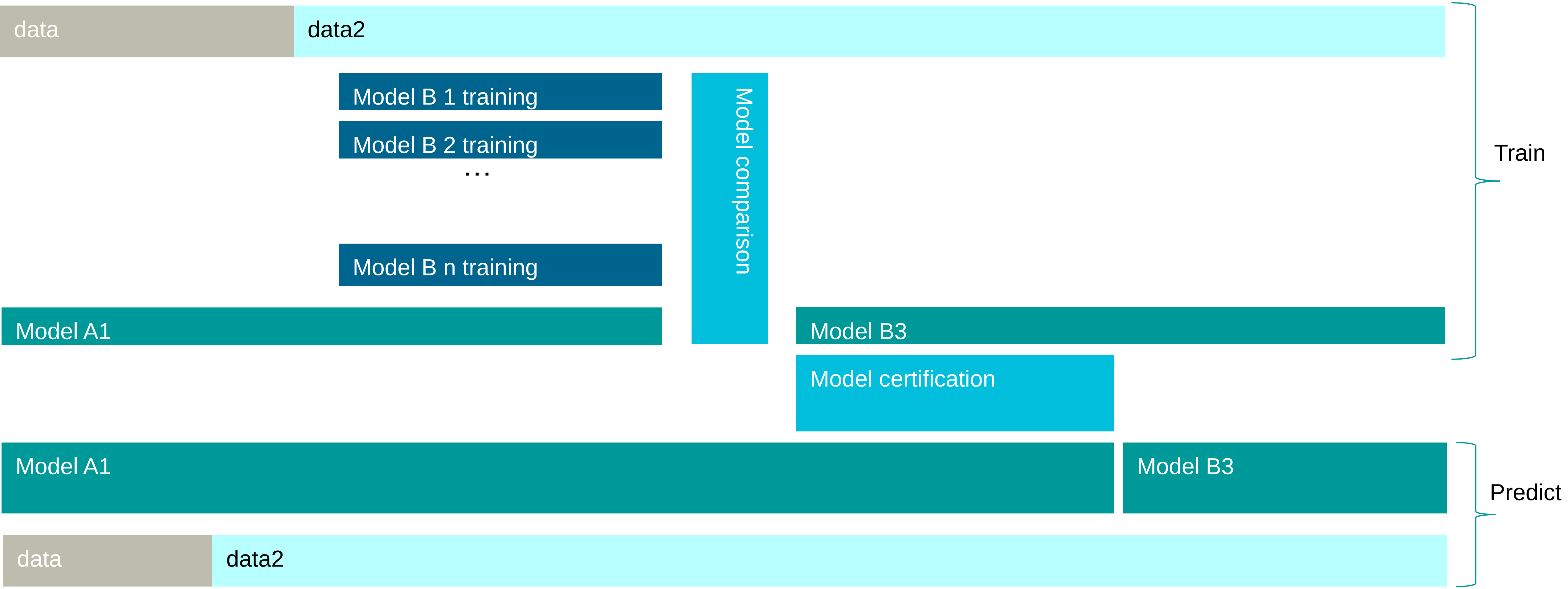
Tensor representation of the dynamic variations of observed metrics are used as the input to a trigger model which identifies conditions that will require a preventive maintenance.

Raw input data



Test

Model lifecycle (continuous updating)



Model lifecycle (continuous updating): Back end of line example

	Trained in 7 products		Trained in 9 products		Trained in 11 products	
Target Label	**Pre MADEin4**	**Post MADEin4**	**Pre MADEin4**	**Post MADEin4**	**Pre MADEin4**	**Post MADEin4**
Metro A from Process A	0.473 ± 0.052	0.473 ± 0.052	0.474 ± 0.027	0.474 ± 0.027	0.472 ± 0.023	0.472 ± 0.023
Metro C from Process E	-0.216 ± 0.172	-0.211 ± 0.169	-0.087 ± 0.063	-0.042 ± 0.042	0.641 ± 0.011	0.646 ± 0.007
Metro A from Process F	0.599 ± 0.074	0.670 ± 0.022	0.424 ± 0.117	0.601 ± 0.086	0.771 ± 0.066	0.829 ± 0.007
Metro C from Process F	-0.309 ± 0.100	-0.294 ± 0.108	0.001 ± 0.001	0.001 ± 0.001	0.880 ± 0.015	0.884 ± 0.018
ETEST	-0.322 ± 0.251	**0.384 ± 0.036**	**0.082 ± 0.199**	**0.574 ± 0.012**	**0.212 ± 0.256**	**0.768 ± 0.006**

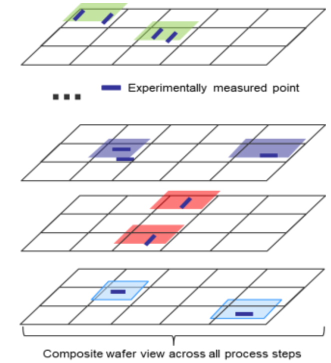
Process analysis discovers metrology steps that contribute the most to explaining Electrical test data.

Pre-MADEin4 indicates state of the art methodology related to virtual metrology

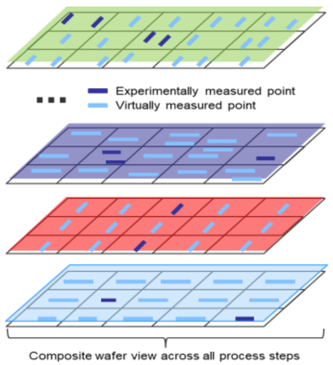
Post-MADEin4 indicates results of using design, metrology and process information of previous process steps to generate a full view of the wafer history.

Score shown is a measure of the percentage of the variability explained by the model, along with a confidence interval.

Pre MADEin4



Post MADEin4



SIEMENS

Model lifecycle (continuous updating): Back end of line example
mean absolute error reduction

	Mean Absolute Error [probe units]					
	7 Product training		9 Product training		11 Product training	
Target Label	Pre MADEin4	Post MADEin4	Pre MADEin4	Post MADEin4	Pre MADEin4	Post MADEin4
Metro A from Process A	17.960 ± 1.027	17.960 ± 1.027	20.610 ± 0.696	20.610 ± 0.696	15.932 ± 0.276	15.932 ± 0.276
Metro C from Process E	1.110 ± 0.089	1.107 ± 0.089	1.327 ± 0.036	1.307 ± 0.025	0.787 ± 0.010	0.783 ± 0.009
Metro A from Process F	0.645 ± 0.050	0.600 ± 0.026	1.112 ± 0.102	0.940 ± 0.103	0.523 ± 0.057	0.467 ± 0.009
Metro C from Process F	5.534 ± 0.352	5.512 ± 0.368	7.585 ± 0.097	7.564 ± 0.106	1.670 ± 0.053	1.624 ± 0.087
ETEST	0.519 ± 0.056	0.321 ± 0.008	0.429 ± 0.052	0.261 ± 0.004	0.354 ± 0.063	0.185 ± 0.003

Thickness Modeling: VERY Low-sample conditions (per wafer)

	LOT 2 :	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21
INSP 2	M2-M1 (OVL & TIS)													V	V						
	V1-M1 (OVL & TIS)													V	V						
	V1-M2 (OVL & TIS)													V	V						

	LOT 2 :	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21
INSP 1	Litho M1 [PW]					V															
	Etch M1 [PW]						V														
	Metallization M1 [POR]				V																
	Litho M2 [PW]									V											
	Etch M2 [PW]										V										
	Metallization M2 [POR]			V																	
	Litho V1 [PW V1]																	V			
	Etch DD V1 [PW V1]																		V		
	Litho V1 [PGD OVL]													V							
	Etch DD V1 [PGD OVL]														V						

	LOT 2 :	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21
OCD	OCD post Litho (resist CD & resist height)					V															
	OCD Post Etch (TRENCH & CD)						V														

	LOT 2 :	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21
THK	M1 Metal				V																
	M1 Litho					V															
	M1 Etch						V														
	M2 Metal			V																	
	M2 Litho									V											
	M2 Etch										V										
	PGD Litho													V							
	PGD Etch														V						
	Via Litho																	V			
	Via Etch																		V		

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Incorporating Inspection measurements to improve thickness prediction

Slot (Wafer)	Metrology		Mean Absolute Error and relative improvement on Thk measurement			
			Spatial only	Thk + Insp 1	Thk + Insp 2	Thk + Insp 1 + Insp 2
D14	**I_AVG_Cu_pad1**		28.186	5.05%	4.56%	4.09%
	I_AVG_Ti_pad1		10.7517	25.51%	33.66%	31.27%
	I_AVG_Cu_pad4		33.1282	-11.08%	-9.75%	-6.52%
	I_AVG_Ti_pad4		9.449	-9.95%	-7.96%	-11.37%
	I_AVG_Cu_pad7		127.5466	-6.22%	-5.76%	-5.67%
	I_AVG_Ti_pad7		7.2792	1.41%	6.53%	5.32%
	I_AVG_Cu_pad15		113.6475	-0.27%	1.75%	-5.90%
	I_AVG_Ti_pad15		7.4108	-11.46%	-1.02%	-3.07%

Slot (Wafer)	Metrology		Mean Absolute Error and relative improvement on Thk measurement			
			Spatial only	Thk + Insp 1	Thk + Insp 2	Thk + Insp 1 + Insp 2
D15	**I_AVG_Cu_pad1**		27.2433	6.68%	1.13%	1.65%
	I_AVG_Ti_pad1		2.4454	-11.15%	-3.03%	-6.88%
	I_AVG_Cu_pad4		35.7732	-9.01%	-8.49%	-11.10%
	I_AVG_Ti_pad4		2.2587	-11.09%	-2.67%	-7.75%
	I_AVG_Cu_pad7		130.0169	-10.70%	-5.77%	-6.94%
	I_AVG_Ti_pad7		2.5341	-0.29%	6.60%	7.06%
	I_AVG_Cu_pad15		109.6425	-5.40%	-4.64%	-0.43%
	I_AVG_Ti_pad15		2.8265	-2.34%	-1.54%	-6.46%

Some thickness values improve while others degrade.

However, improvement or degradation on the model quality under low-sample conditions is an indication that other effects may be present that need to be accounted for.

Electrical Test Modeling: Small Sample conditions (21 wafer lot)

	LOT 1 :	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21
IMEC	Stack Ellipsometry	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	M1 post-Litho CDSEM	V	V		V					V					V						
	M1 ADI (asymmetry and shifts)	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	M1 post-Etch CDSEM	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	M1 post CMP Scatterometry	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	M1 post CMP (asymmetry and shifts)	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	M2 post-Litho CDSEM	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	M2 post-Etch CDSEM	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	V1 post-Litho CDSEM					V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	V1 post-Etch CDSEM	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	Overlay measurements M1, M2, V1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	Electrical measurements	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

Most wafers are measured using every available metrology at every process step.

This permits the learning across multiple wafers within the lot.

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Electrical Test Modeling: Improvements in ETEST characterization

Electrical Target	Pre-MADEin4	Post-MADEIn4	Error Reduction
ETEST 1	0.00444	0.00421	5.18%
ETEST 2	2.99781	1.74479	41.80%
ETEST 3	5.35082	4.3712	18.31%
ETEST 4	66.96937	63.16391	5.68%
ETEST 5	64.37485	59.98278	6.82%
ETEST 6	53.30767	49.9263	6.34%
ETEST 7	50.8815	48.86645	3.96%
ETEST 8	147.55088	148.18903	-0.43%
ETEST 9	113.61041	115.0878	-1.30%
ETEST 10	0.00536	0.0054	-0.75%
ETEST 11	0.48307	0.4765	1.36%
ETEST 12	5.71922	5.32819	6.84%
ETEST 13	4.42041	3.88363	12.14%

Some electrical targets exhibit no benefit, while most electrical tests see a reduction in the mean absolute error for all samples

The explain ability analysis identifies measurements and process steps contributing the most to process characterization of the electrical response of the manufacturing process

	ETEST1	ETEST2	ETEST3	ETEST4	ETEST5	ETEST6	ETEST7	ETEST8	ETEST9	ETEST10	ETEST11	ETEST12	ETEST13
Stack Ellipsometry											V		
M1 post-Litho CDSEM													
M1 ADI (asymmetry and shifts)	V	V	V	V	V	V	V	V	V	V	V	V	V
M1 post-Etch CDSEM					V	V	V					V	
M1 post CMP Scatterometry	V	V	V	V	V	V	V	V	V	V	V	V	V
M1 post CMP (asymmetry and shifts)	V	V	V	V	V	V	V	V	V	V	V	V	V
M2 post-Litho CDSEM						V	V	V					
M2 post-Etch CDSEM		V		V	V			V	V		V	V	
V1 post-Litho CDSEM				V	V	V		V	V	V			
V1 post-Etch CDSEM				V		V		V	V	V	V	V	V
Overlay measurements M1, M2, V1	V			V	V	V		V		V	V	V	

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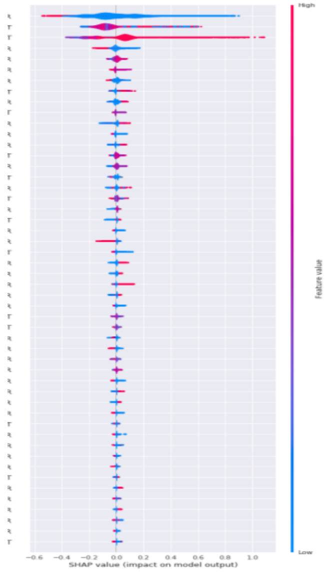
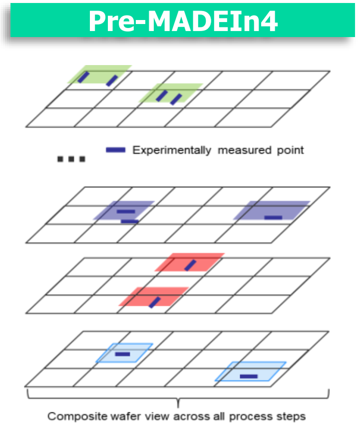
Electrical Test Modeling: Large Sample Size conditions (Thousands of wafers)

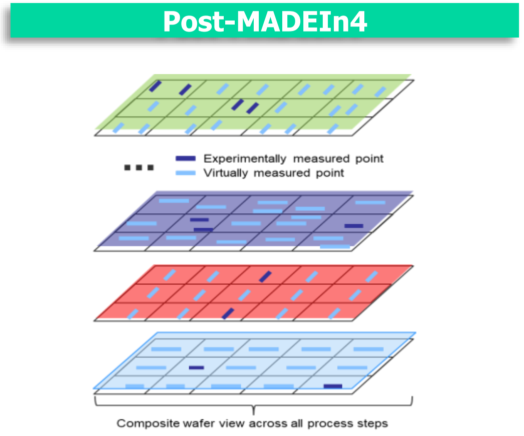


Full process analysis defines probes (intermediate inline measurements that contribute the most to final target accuracy)

Benefit of Design features aids in intermediate probes, which in turn reduce the uncertainty of the predictions.

However, the major benefit is found in the application of the cross-metrology technique which enables full stack characterization.





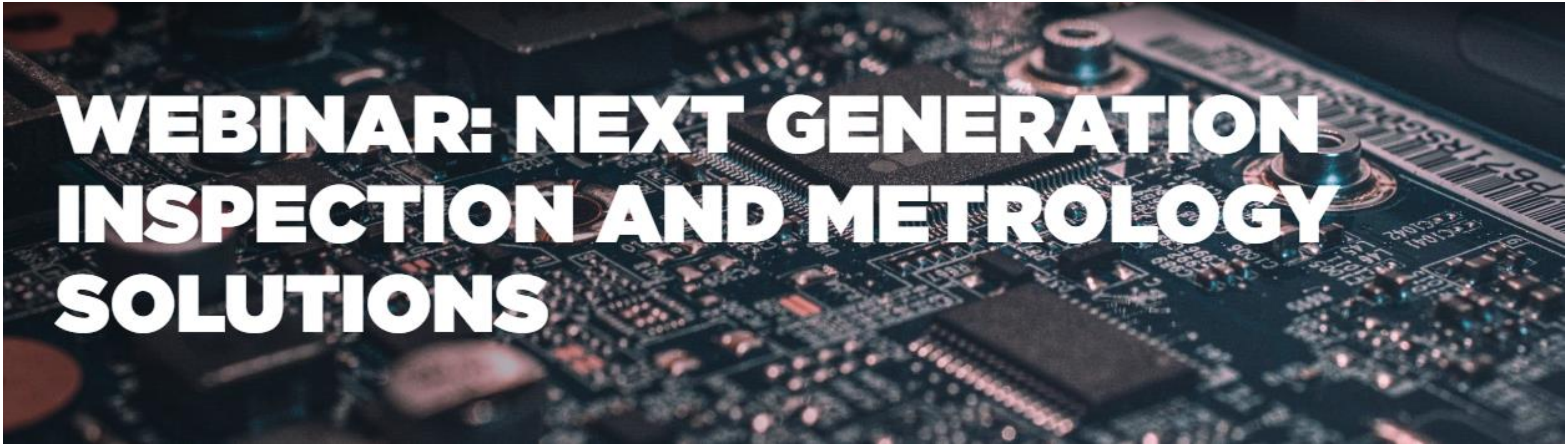
Mean Absolute Error			
Probes and Targets	**Pre-MADEin4**	**Post-MADEin4**	**Error Reduction**
Thickness measurement for process A	15.932 ± 0.276	15.932 ± 0.276	0.00%
Overlay measurement for process B	0.787 ± 0.010	0.783 ± 0.009	0.51%
CD Measurement for process C	0.523 ± 0.057	0.467 ± 0.009	10.71%
CD Measurement for process D	1.670 ± 0.053	1.624 ± 0.087	2.75%
Electrical TEST	0.354 ± 0.063	0.185 ± 0.003	47.74%

Acknowledgements

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826589. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, Italy, Austria, Hungary, Romania, Sweden and Israel

We also want to recognize the fantastic efforts by MADEin4 partners, specially GlobalFoundries, Applied Materials, ST, Bruker, NOVA, IMEC and KLA.

MADEin4



Industry4.0 productivity improvement in major EU fabs

Presenter: Daniele Pagano
STMicroelectronics

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Outline

- MADEin4 project
- Improvement of DoE procedures
- Developments on metrology tools
- Advancement on Process Control
- Predictions on maintenance
- Data Interoperability for Predictive Maintenance
- Conclusions and Opportunities

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MADEin4 project

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MADEin4 Consortium

- Number of consortium members: 47. Countries involved:10
- Start date: April 1, 2019. Duration: 36 months + 6 months extension
- Total effort: person months: 10,503 (875 person years)

Coordinator – AMIL

Ilan Englard - Primary contact

Gerold Alberga - Coordination support

Work Packages Leaders

Ilan Englard - AMIL - WP1

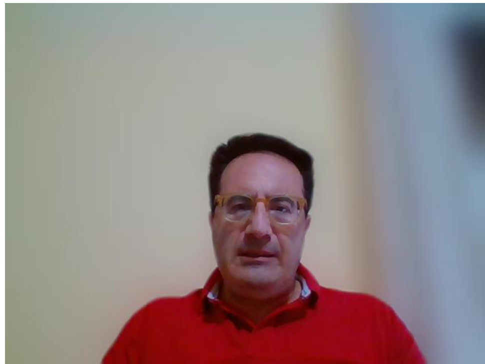
Rudi De Ruyter - IMEC - WP2

Frank de Jong - FEI (THERMO FISHER) - WP3

Andres Torres - MENTOR - WP4

Daniele Pagano - ST ITALY - WP5

Olaf Kievit - TNO - WP6



MADEin4 WP5: Industry 4.0 digitization of manufacturing

Task 5.1 - Digitization of ECS (Electronic Components and Systems) manufacturing (ST-I, CNR, POLITO, MELLANOX, MENTOR, TNO, PTB, SEMIL, EXCILLUM)

Task 5.2 - Digitization of Automotive manufacturing (FCA-ITALY, COMAU, POLITO, AVL, BRIL, NM, TOWER, TUD, DITEST, VIF)

WP1	WP2	WP3	WP4	WP5	WP6
Management (AMIL)	Requirements, samples and Industry 4.0 pilot line infrastructure (IMEC)	Metrology platform developments for enhanced productivity (THERMO)	Industry 4.0 predictive yield and tools performance pilot line for enhanced productivity (MENTOR)	Industry 4.0 digitization of manufacturing for enhanced productivity (ST IT)	Standards, dissemination and exploitation (TNO)
T1.1 Administration and financial co-ordination (AMIL)	T2.1 Metrology requirements (IMEC)	T3.1 Metrology for Semiconductor manufacturing (THERMO)	T4.1 Predictive Yield for Semiconductor and Automotive manufacturing (MENTOR)	T5.1 Digitization of Semiconductor manufacturing (ST IT)	T6.1 Metrology Standards (PTB)
T1.2 Project management and Technical co-ordination (AMIL)	T2.2 Design and fabrication of metrology samples (IMEC)	T3.2 Metrology for Automotive manufacturing (AVL)	T4.2 Predictive tools performances and availability for Semiconductor and Automotive manufacturing (THERMO)	T5.2 Digitization of Automotive manufacturing (FCA)	T6.2 Industry 4.0 Standards (COMAU)
T1.3 Communication management (AMIL)	T2.3 Industry 4.0 pilot line operation and Cost Of Ownership (AMIL)		T4.3 Computing platforms for fast data acquisition and analytics (PRODRIVE)		T6.3 Dissemination and exploitation (SEMI EU)
T1.4 Risk management (AMIL)					

Samples

Measurements, data and joint case studies

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WP5: Collaboration and Interaction with other WPs

WP2

Contribution on Metrology Survey

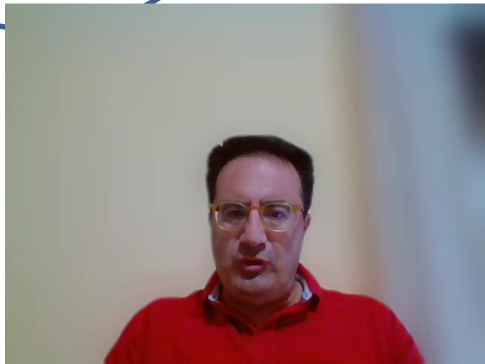
WP5

WP6

All Metrology Companies

WP3

WP4



MADEin4 WP5: Industry 4.0 digitization of manufacturing

Work Package 5: main objectives

- Adaptation and implementation of MADEin4 solutions in automated manufacturing lines characterized by:
  - large volume of global production
  - already achieved high level of efficiency
  - lots' management aiming at the products' development or products' customization

- The goal is to increase yield of the entire production process (Semiconductor and Automotive), integrating the use of **IoT methods**: innovative metrology tools, control/implementation tools and advanced calculation/simulation methods.

MADEin4 WP5.1: Digitization of Semiconductor Manufacturing

- **Task 5.1.1 Improvement of the <u>Design of Experiments (DoE)</u> procedures for manufacturing process optimization**
  - Use case 1: SiC trench plasma etching process
  - Use case 2: Laser annealing of Ni-SiC systems for back-junction formation
  - Use case 3: Thermal curing after Cu Electrochemical Deposition as back-end process
- **Task 5.1.2 Acceleration of the operating protocols for the <u>process control</u>**
  - Use case 4: In-line Contamination monitoring by of X-ray spectroscopy on Silicon Carbide substrate
  - Use case 5: Virtual Metrology to eliminate test wafers measurements on electroplating deposition of Cupper
- **Task 5.1.3 Data analytics for <u>predictions</u> of the power production line**
  - Use case 6: Predictive Maintenance of the ECD equipment for Cu deposition
  - Use case 7: Predictive Maintenance of Chemical Oxide Deposition (CDO)

  equipment for oxide deposition
  - Use case 8: Auto defect classification of BCD/MEMS Technologies

Improvement of DoE procedures

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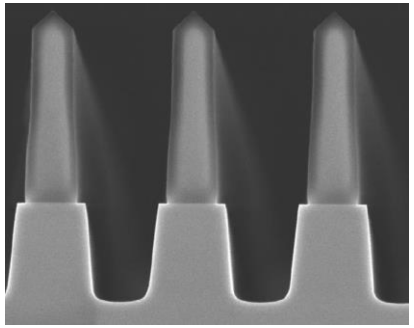
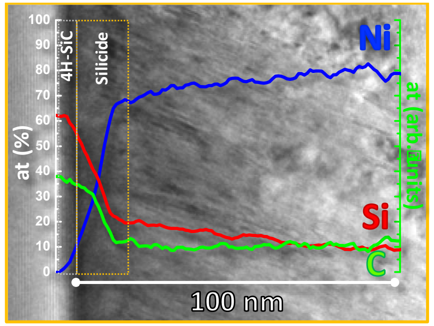
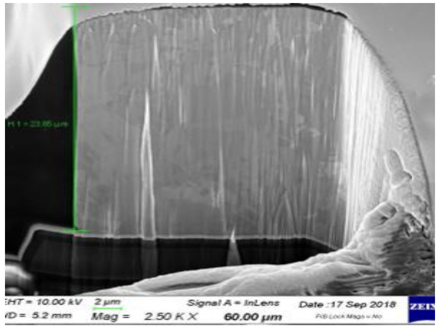
Improvement of the Design of Experiments (DoE)



UC1 SiC Trench plasma etching process setup



UC2 SiC-Ni Silicide laser formation process set up



UC3 Thick Cu Electroplating deposition process set up

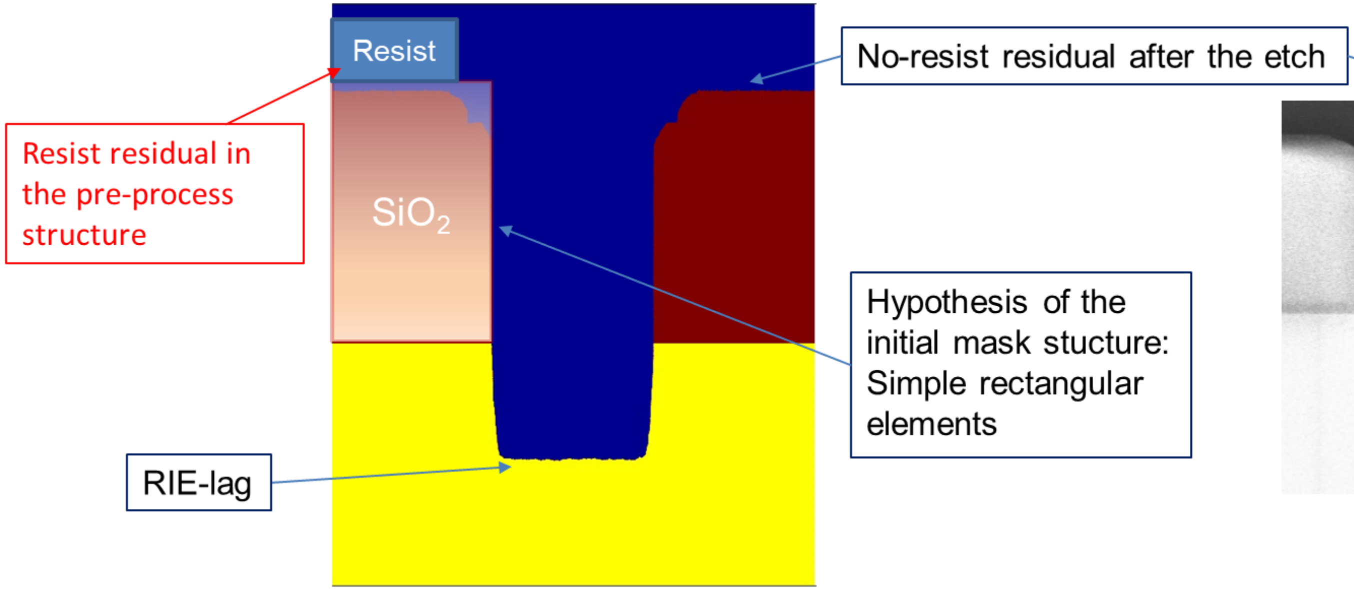
Design of Experiments (DoE) speed-up by integrating real experiments (R-DoE) and non-destructive characterization of processed samples, as virtual DoE (V-DoE)

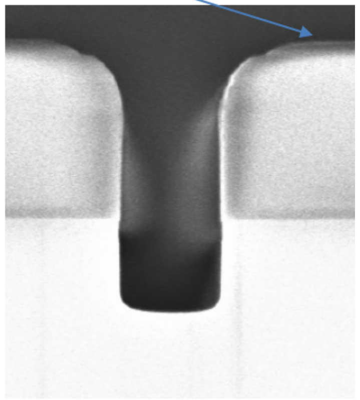
The final goal, lain in the validation of the simulation result, with a minimal use of R-DoE and the possible expansion in a very large number of conditions with affordable use of CPU resources,

thanks to V-DoE approach has been fully achieved.

UC1 - SiC trench plasma etching process

CNR developed simulation codes, based on Monte Carlo method and realized V-DoE. Further characterizations of processed samples were included to integrate ST’s measurements.



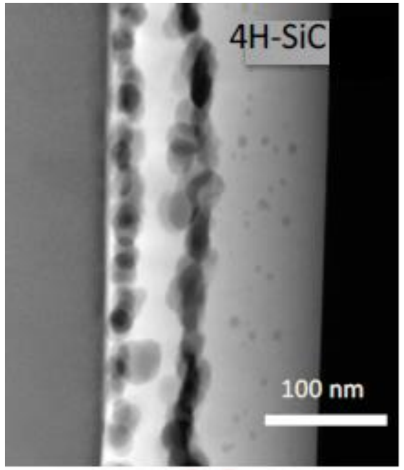


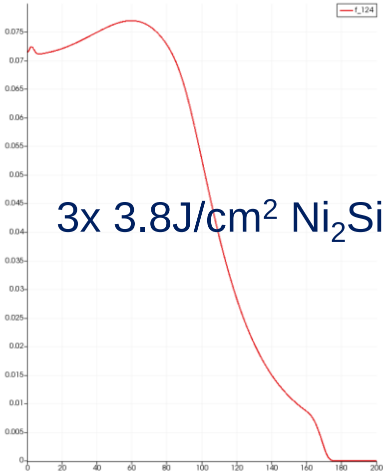
Accurate predictions: SiC+hard mask evolution during plasma exposition

ST-I and CNR demonstrate virtual DOE improvement for plasma etching of SiC by simulating several process conditions and target was reached by decreasing the number of physical iteration by factor of 10.

UC2 - Laser annealing of Ni-SiC systems for back-junction formation

3x 3.8J/cm^2 STEM





Combined Virtual and Real DoE procedure extended in the multi-pulse conditions in collaboration with UPB

Low Rs is achieved with no evidence of transition to the low resistivity NiSi phase

Mixture of Ni-rich silicides and C-clusters

No residual of Ni-Si alloy (with high resistivity) and increased uniformity are the critical features for the optimal conditions

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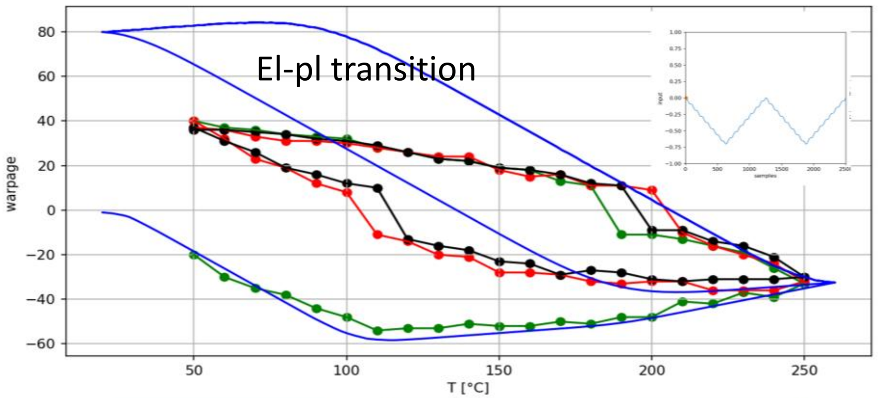
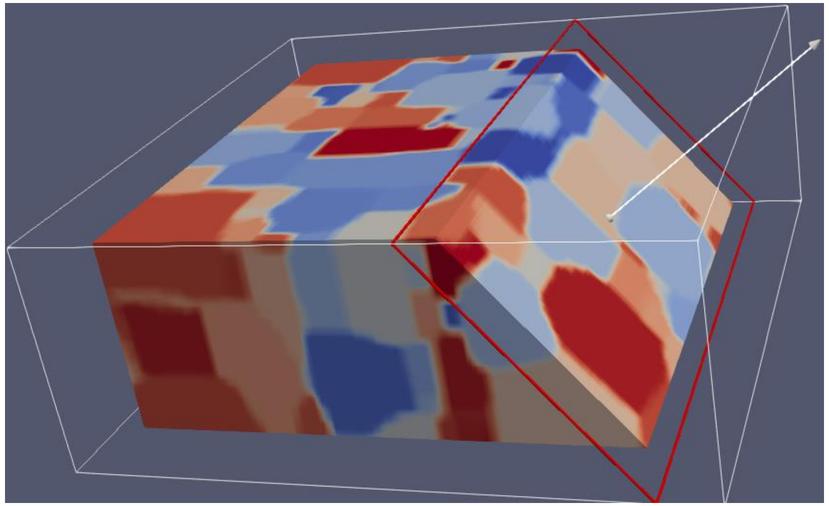
UC3 - Thermal curing after Cu Electrochemical Deposition as back-end process

2 cycles



Elastic bahaviour

Densification elasto-plastic transition



- Understanding of the warpage behavior in term of a transition to Preisach elastoplastic approach
- The same local stress field is can be transferred from small sample to the wafer scale to understand global deformation
- Combined Virtual and Real DoE study to find optimal thermal cycle condition in term of microstructure and warpage control
- KPI achieved by integration of V-DoE and R-DoE:
  - Destructive analysis rate: 10% of the trials
  - V-DoE can be expanded in a x100 conditions (DoE points) with respect the R-DoE points
  considered in the validation in about 500h of computation

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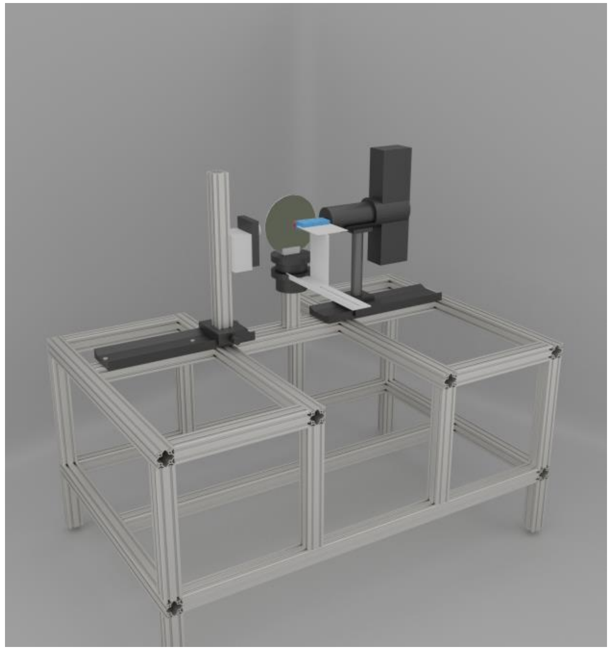
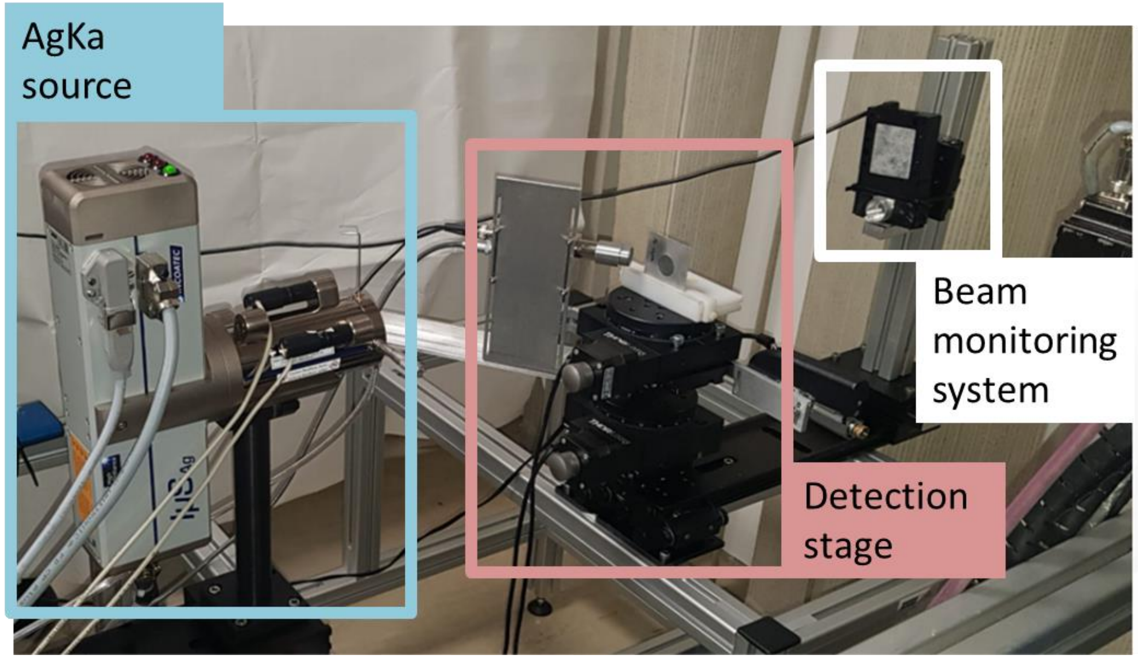
Improvement of the DoE procedures

Code Accuracy > 95% (UC1,UC2,UC3)	☺ Verified, considering also experimental intrinsic variability of the processes
Very limited number of samples which are subjected destructive characterization analyses (UC1,UC2,UC3)	☺ OK. The number of distroyed samples/wafers for the code validation is very low
DoE Complexity ~100 trials (UC1,UC2,UC3); Destructive analysis rate: 50% of the trials. (UC1), Destructive analysis rate: 5% of the trials. (UC2), Destructive analysis rate: 10% of the trials (UC3)	☺ ☺ **V-DoE can be expanded in a x100 conditions (DoE points) with respect the R-DoE points considered in the validation in about 100h, 300h, 500h of computation for the UC1, UC2, UC3 respectively**

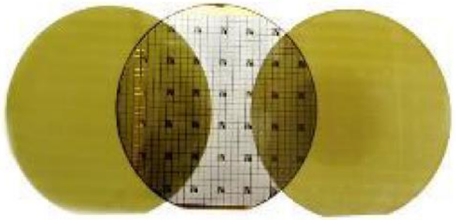
Developments on metrology tools

Acceleration of the operating protocols for the process control





SiC Wafers



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BRUKER

excillum

PTB

Proof of Concept: first laboratory prototype

Realization and testing of high precision laboratory prototype employing a high brilliance (~108 photons/sec) low convergence (~ 0.3 deg) monochromatic Cu Ka source with significant acquisition time reduction and higher sensitivity.

Advancement on Process Control

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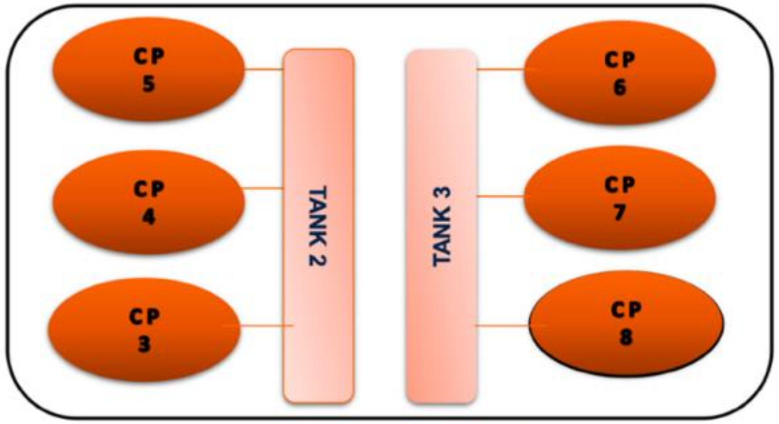
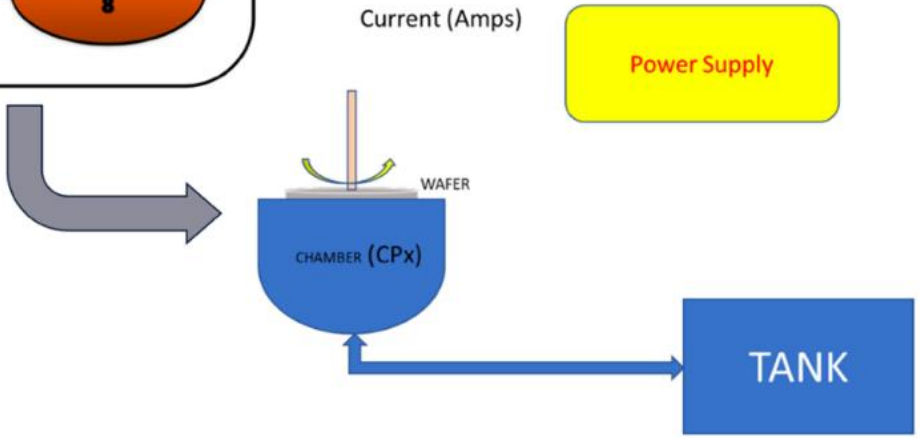
Virtual metrology on Copper ECD





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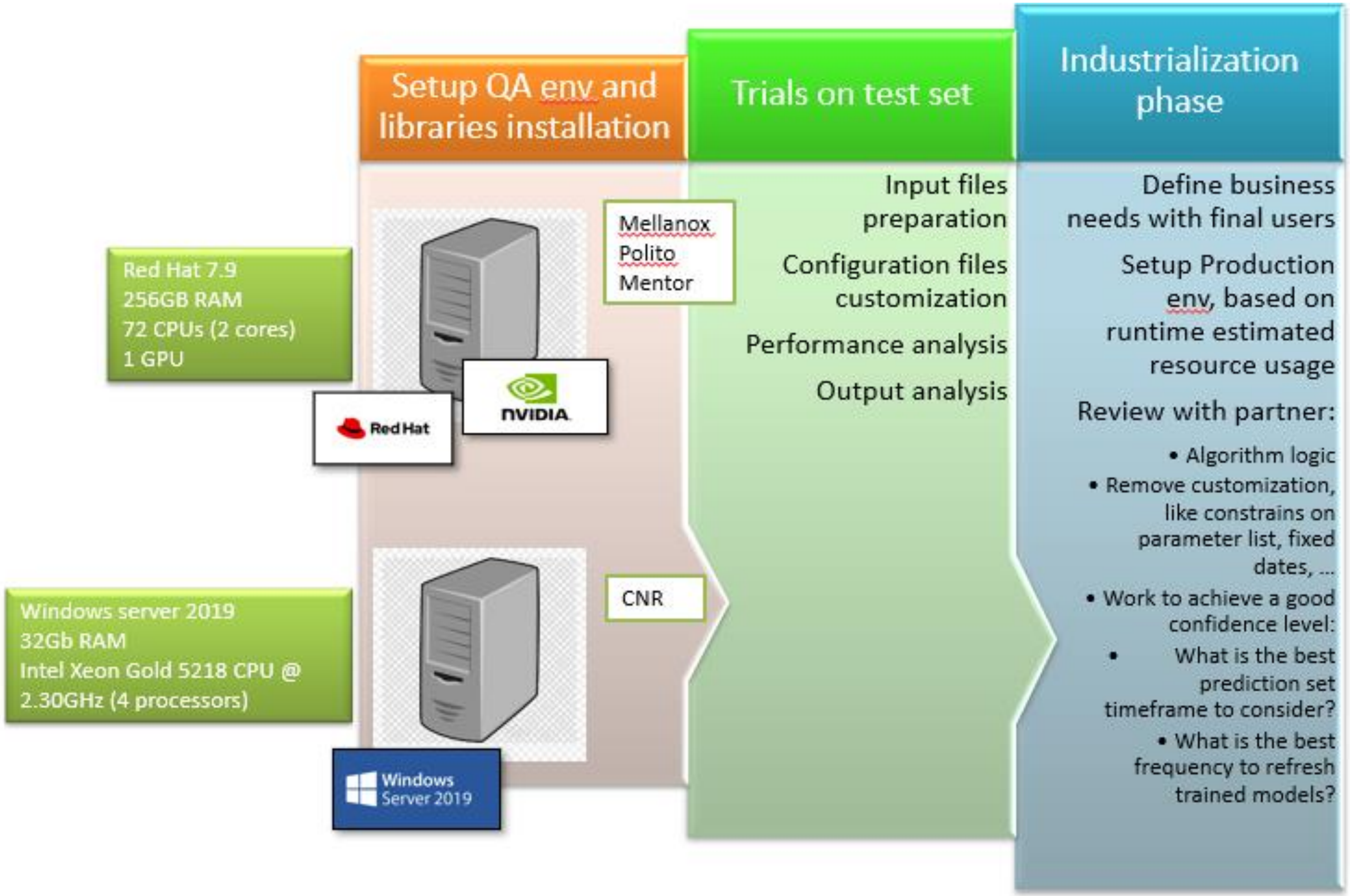
Each partner developed own algorithm, after evaluating several methods and approaches and above all sharing ideas and results. These algorithms will allow to add virtual measurements to all wafers belonging to the same lot, finally to reduce the sampling frequency

Virtual metrology to eliminate test wafers measurements on electroplating deposition of copper



In the implementation phase different architecture are got ready in demo environment

Prediction accuracy is under evaluation for each software

Significant information are collected regarding architecture efficiency also

Predictions on maintenance

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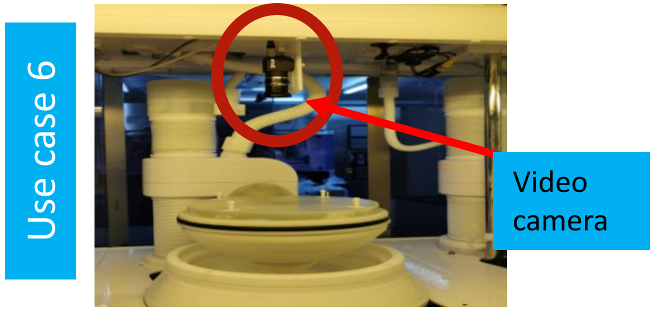
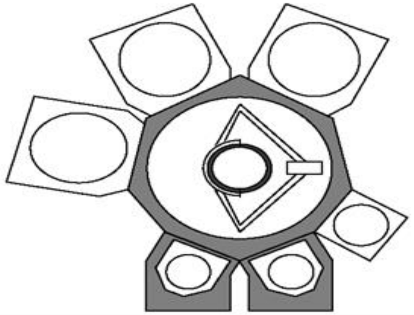
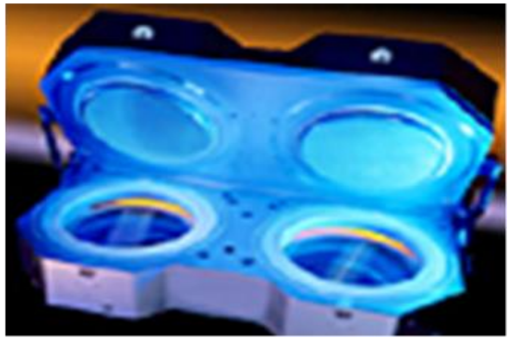
Predictive virtual processes, metrology and maintenance in power device manufacturing



UC6 predictive maintenance of the ECD equipment for Cu deposition

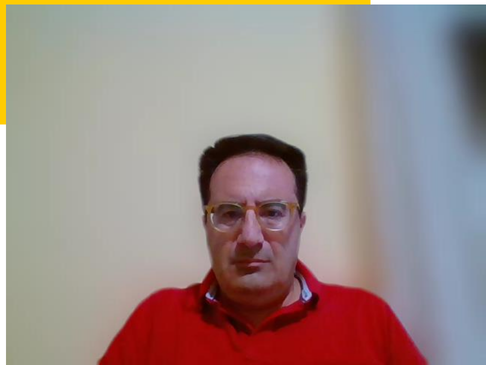




UC7 predictive maintenance of Chemical Oxide Deposition (CDO) equipment for oxide deposition

Predictive Maintenance (PdM) is accomplished through acquiring relevant equipment and factory data and applying an equipment degradation model to predict the equipment's remaining useful life (RUL).

ISMI International SEMATECH Manufacturing Initiative Technology Transfer #10105119A-TR



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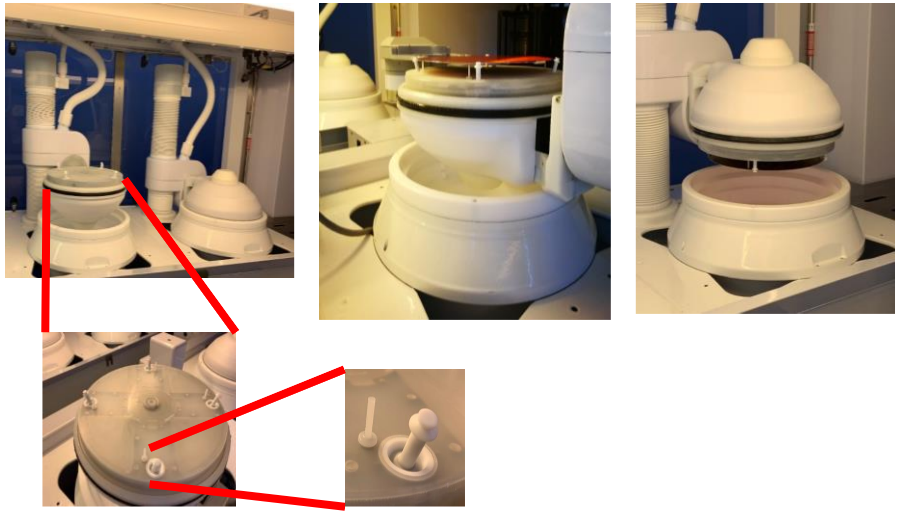
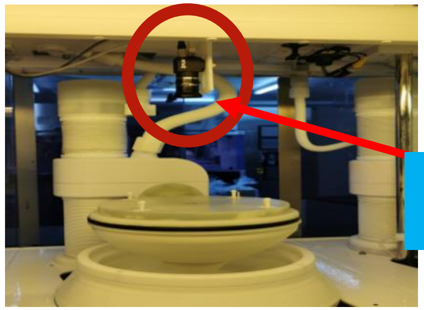
Predictive maintenance of the ECD equipment for Cu deposition

Copper Electroplating Deposition Equipment

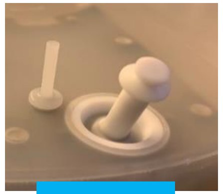


Copper Electrodeposition chamber details, showing wafer holding mechanism by pins.

Use case 6



Video camera



pins

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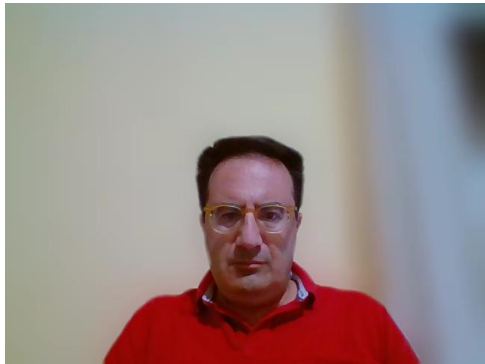
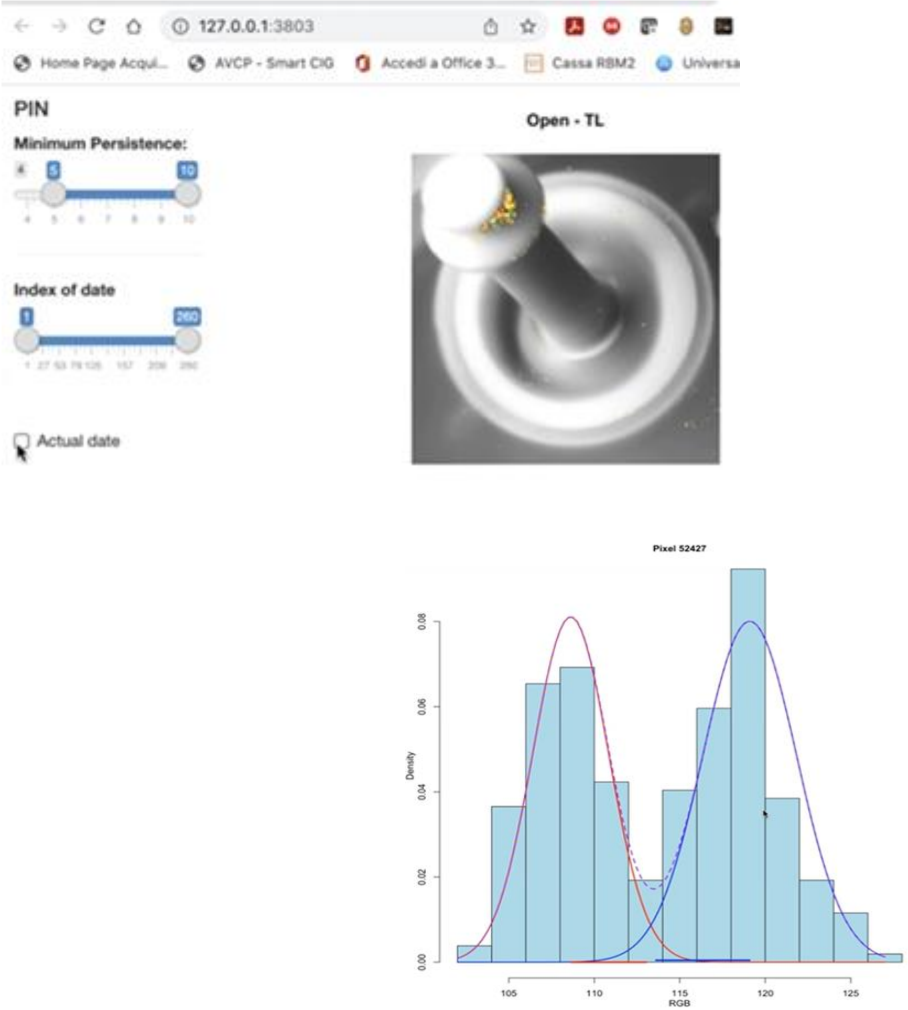
life.augmented

Consiglio Nazionale delle Ricerche

Mellanox



Predictive maintenance of the ECD equipment for Cu deposition



The pins degradation occurs suddenly, so a severe damage of wafers and chamber can occur, as corrosive chemicals are used during the process

At beginning the pins were replaced even if still in good conditions on fixed calendar-based schedule. Therefore, this approach caused extra cost of spare-parts and labor

Currently, the algorithms are capable to catch anomalies.

Thanks to this approach the pins replacement was modified from time based to video-camera one

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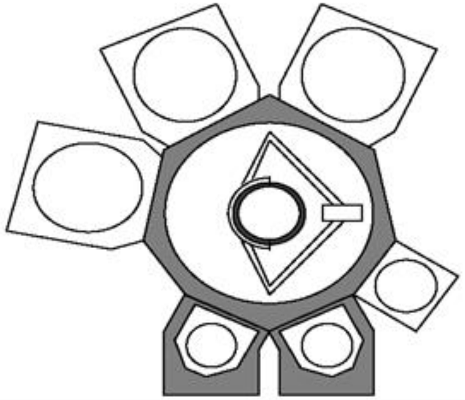
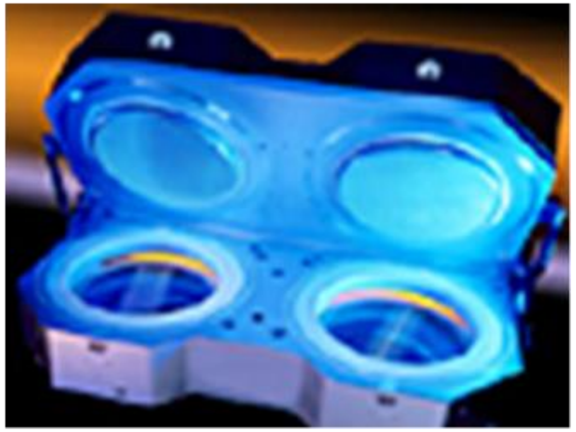
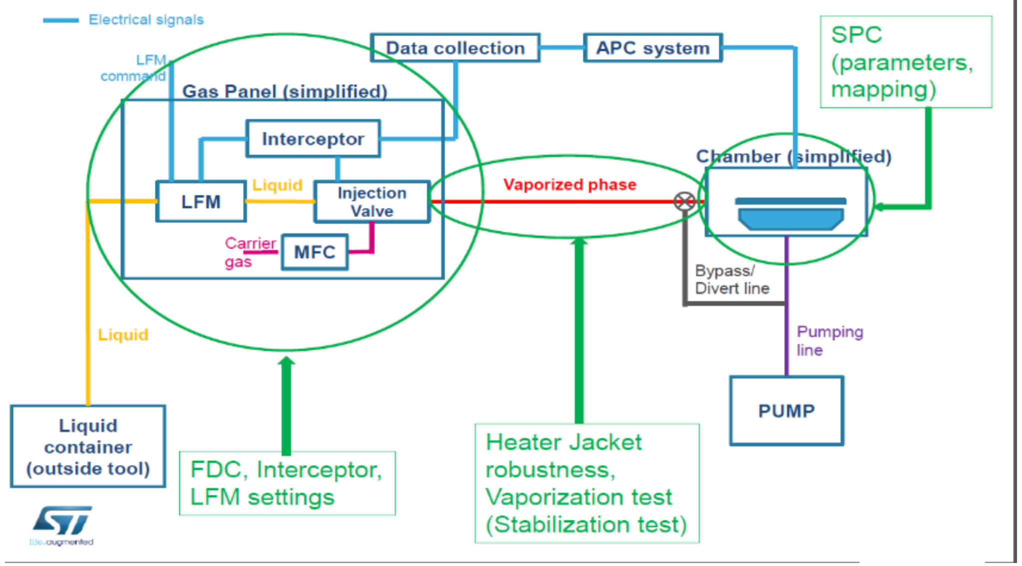
Predictive maintenance of Chemical Oxide Deposition (CDO) equipment for oxide deposition





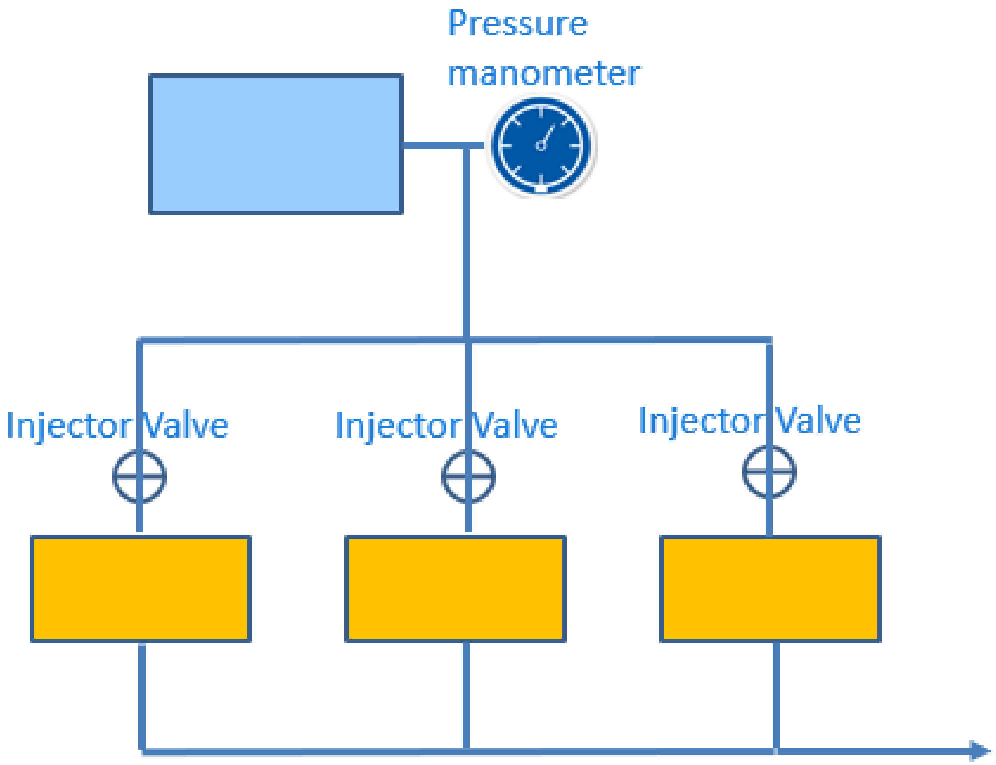
Centura platform (left), Producer platform (right)

Chamber/process securization



The CVD (Chemical Vapor Deposition) process includes a mixture of TEOS ($Si(OC_2H_5)_4$ liquid precursor) and helium (vapor carrier).
The Injection Valve that controls the TEOS flow, is one of the most critical part of the system, as clogs with time, resulting in a flow reduction.

Predictive maintenance of Chemical Oxide Deposition (CDO) equipment for oxide deposition



Algorithms are capable to catch these clogs and TEOS flow reduction in advance

The algorithms are running in demo environment for tuning accuracy and standardize the output's format

Preliminary results are promising to introduce PdM

Data Interoperability for Predictive Maintenance

Synergies: Data Interoperability for Predictive Maintenance

- **Two real case study are selected and shared between IPPON and AVL:**
  - To demonstrate the data interoperability between two different domain and to overcome the state of art paradigm that bound each solution in its product domain
  - As preliminary step before starting an effective cross fertilization, Partners discovered some hidden assumptions and specific approaches used in the two different domains
  - Both approaches were analyzed, and confirmed the effective room for cross fertilization and exploitation

The Epsilon® 2000
World's first production single wafer epi reactor

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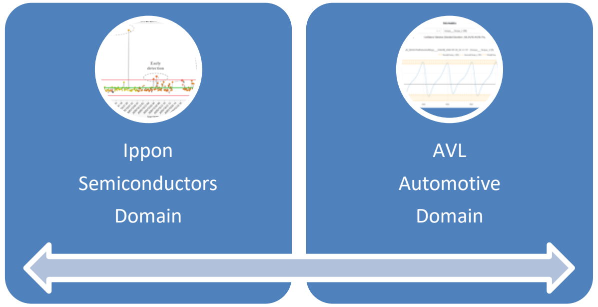


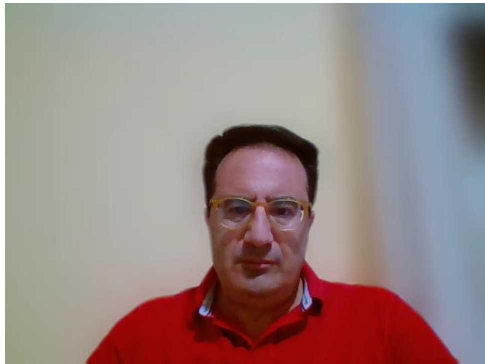
ippon

AVL

Engine Test bench

FCA
FIAT CHRYSLER AUTOMOBILES

Conclusions and Opportunities



Conclusions and Opportunities

MADEin4 Consortium

Metrology Advances for Digitized ECS industry 4.0

Open discussion among partners discovered some **hidden assumptions and specific approaches** used in the different domains

Sharing ideas and computing on real production data

New advanced solutions developed and implemented in semiconductor manufacturing to speed up new products qualification and improve equipment availability by reducing the Cost of Ownership

Embed VM for improving quality data analysis and optimizing process control

New reusable approaches
for investigating innovative processes

ECSEL Joint Undertaking
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Acknowledgments

A special thanks to all researchers involved in these topics

The authors thank the project MADEin4 (Metrology Advances for Digitized Electronic Components and Systems Industry 4.0) that has received funding from the ECSEL-JU under grant agreement No 826589.

MADEin4 web page: (https://madein4.eu/)

MADEin4

רשות החדשנות
Israel Innovation Authority

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TOWERJAZZ
The Global Specialty Foundry Leader

MADEin4
Industry 4.0 Digitization of Manufacturing for Enhanced Productivity

Yoav Hirsch, Tower Semiconductors Ltd
Aug. 2022

(Rev 1.0)

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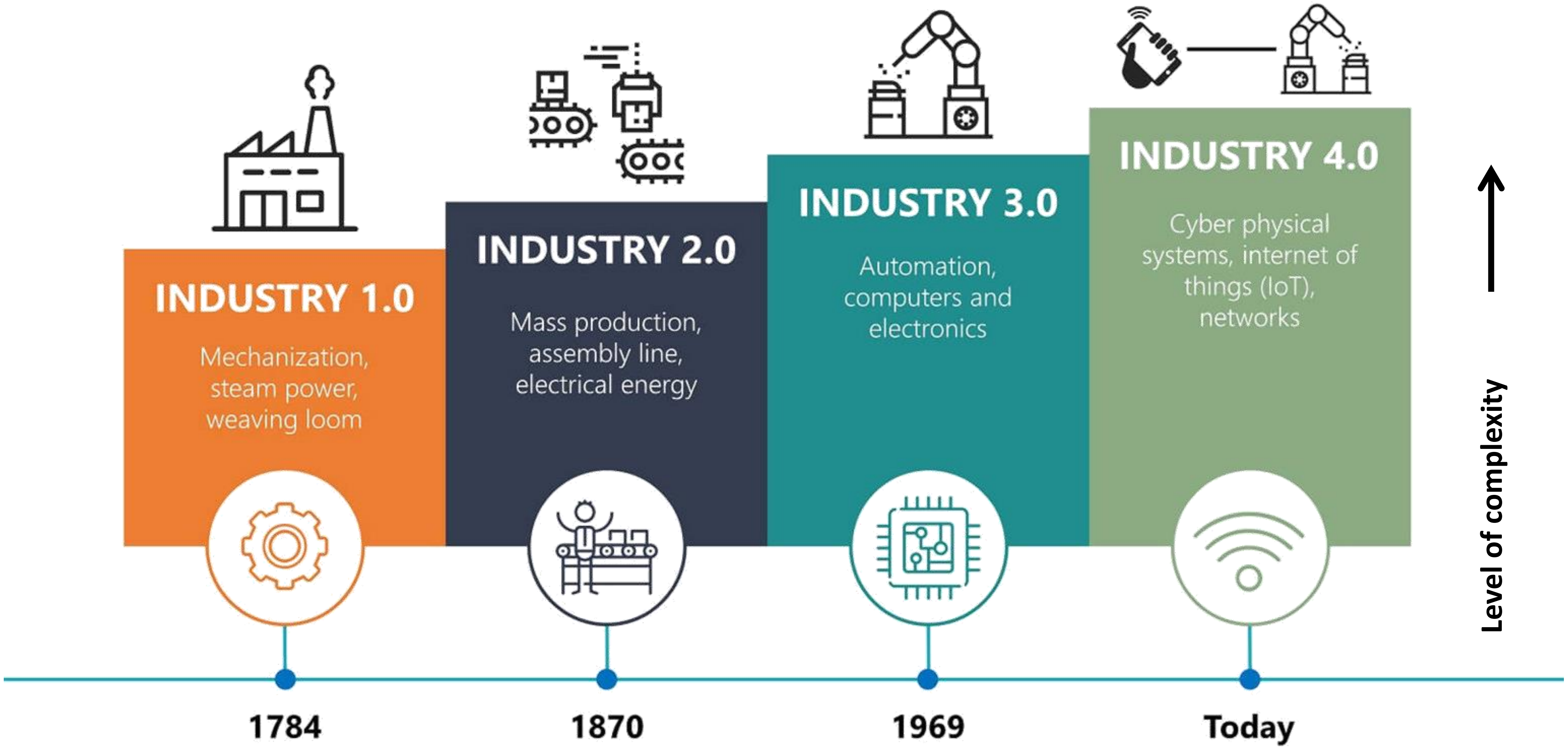
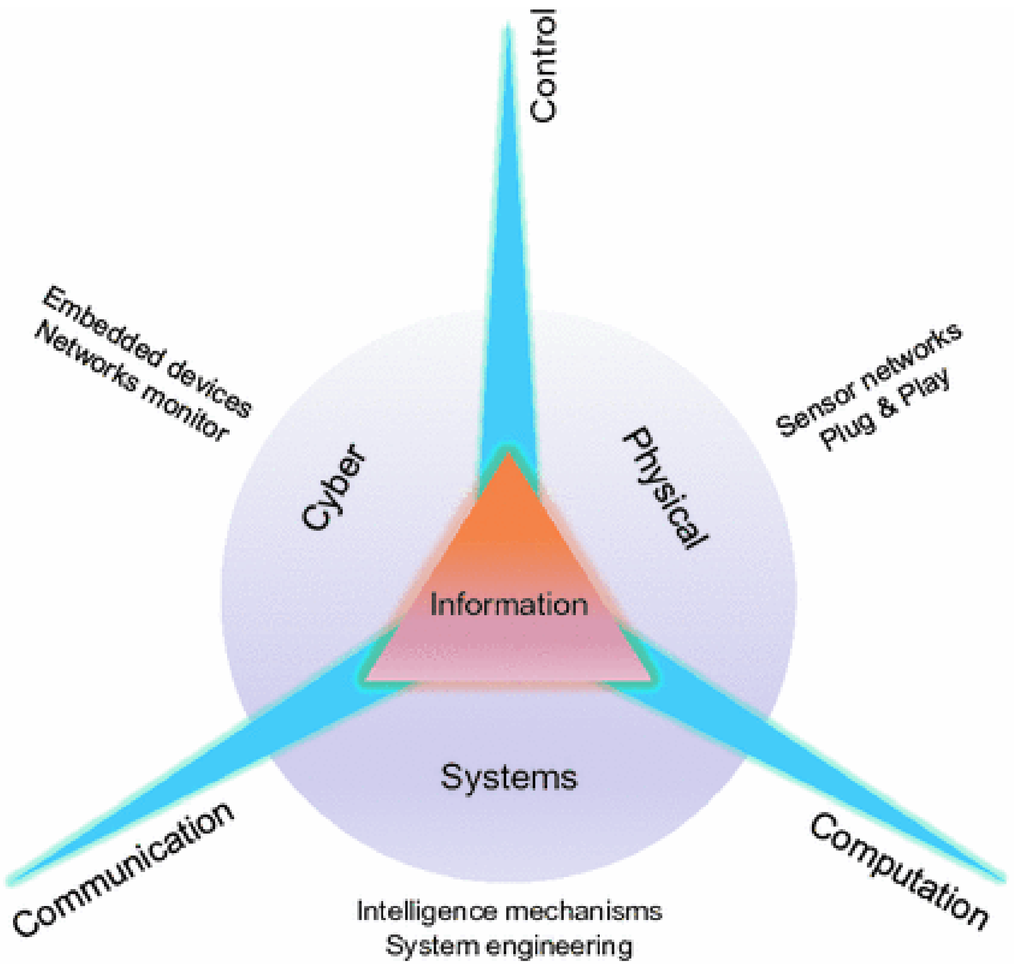
- Industry 4.0
- Semiconductor Manufacturing Metrology
- Machine vision
- Advanced Sensors

TERMINOLOGY: Industrial Revolution



TERMINOLOGY: Cyber-physical Systems (CPS)

The interaction of physical and computing, including embedded intelligence at all levels



MADEin4

Data collection – The new “OIL”

1

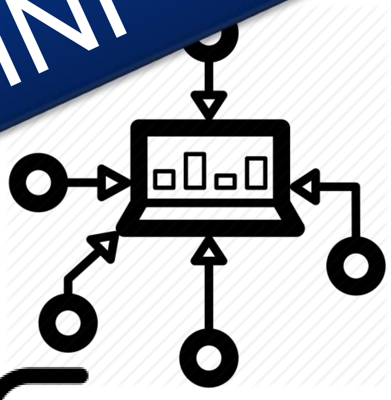
Data collected and pushed to the cloud

2

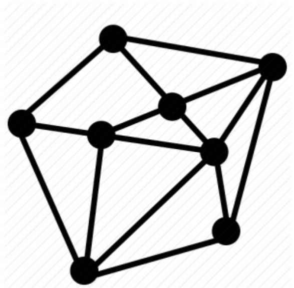
Sensors are added to industrial computers

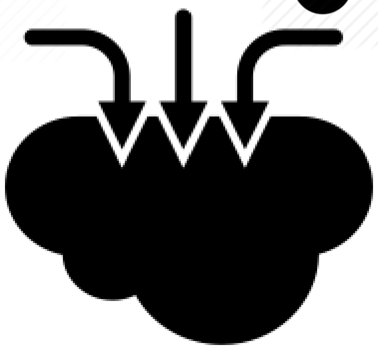
3

Constant data ... for fu...



Data analysis by tailor-made algorithms



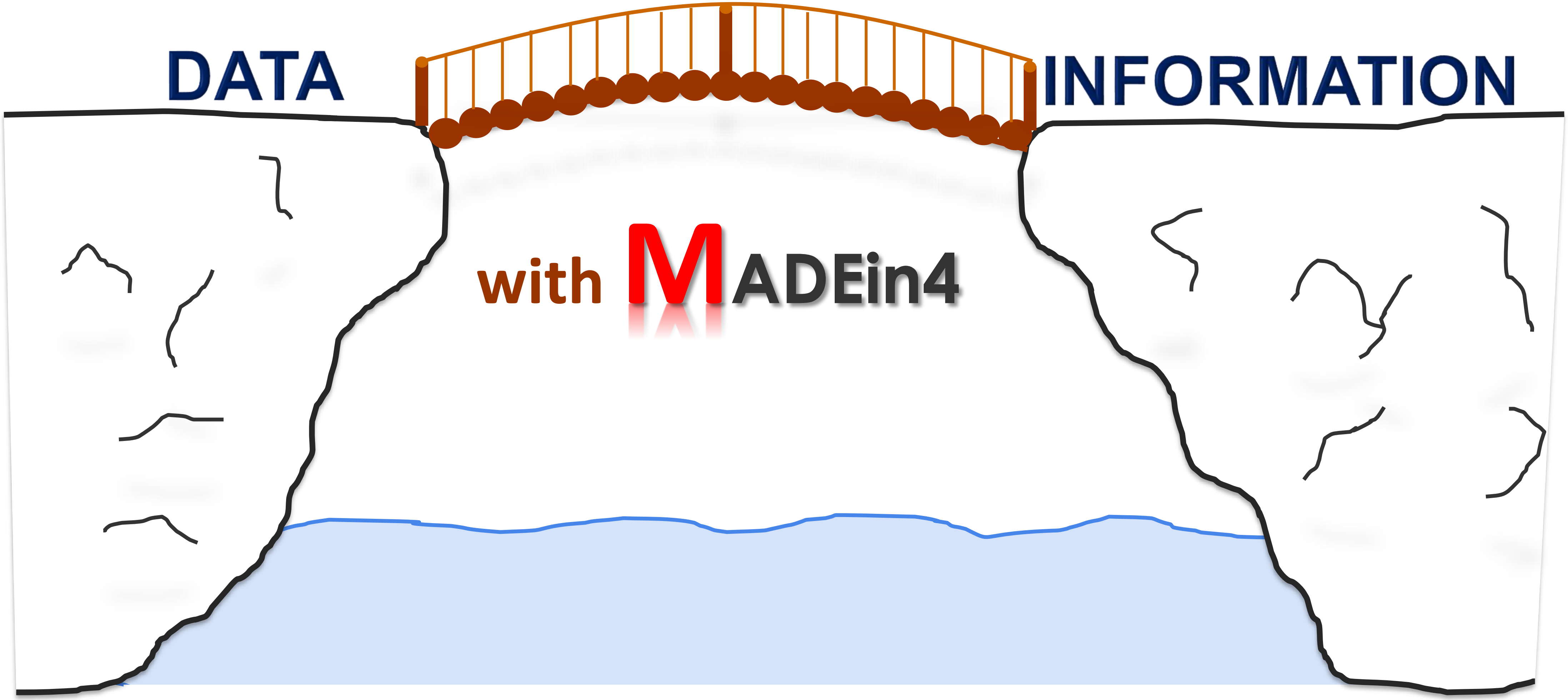


How to convert data to INFORMATION?

INFORMATION =

DATA + **CONTEXT**

CONTEXT (crossing) the chasm



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THANK YOU

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826589. The JU receives support from the European Union's Horizon 2020 research and innovation program and Netherlands, Belgium, Germany, France, Italy, Austria, Hungary, Romania, Sweden and Israel